Universidad Simón Bolívar

LPNHE PARIS

Preparation of the pre-production phase of a detector unit assembly for a High Granularity Timing Detector (HGTD) for the ATLAS detector

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LA-CoNGA physics

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Points to discuss:

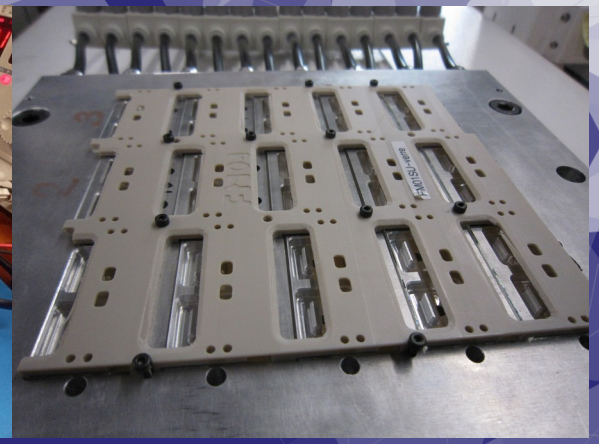
1. Introduction

2. Experimental Framework
   - -High Luminosity LHC (HL-LHC)
   - -High Granularity Timing Detector (HGTD)
   - -Low Gain Avalanche Detector (LGAD)

3. Methodological Framework
   - -Experimental Setup

4. Results and Analysis

5. Conclusions



Introduction: HL-LHC

-Luminosity: Magnitude proportional to the number of collisions on a certain period of time [1].

$$\mathcal{L} = \frac{1}{\sigma}\frac{dN}{dt}\ [\mathrm{cm}^{-2}\mathrm{s}^{-1}],$$

-Pile Up: Abrupt increase in the number of collisions per bunch of crossing particles. σ is the crossed area [1].

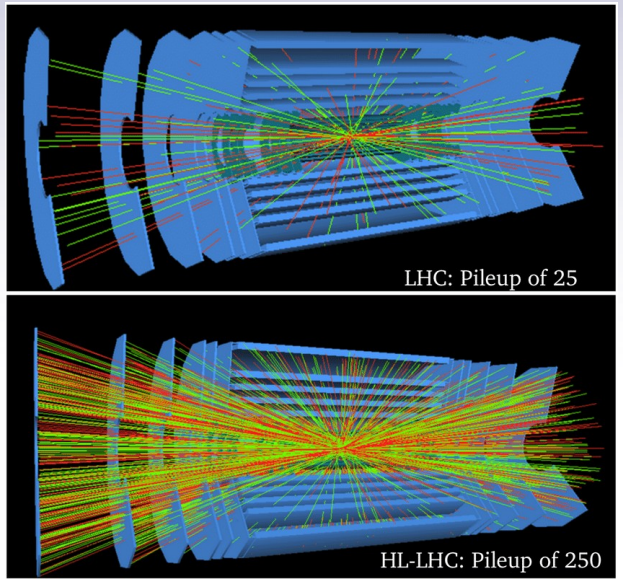


Figure 1: Pile-Up.

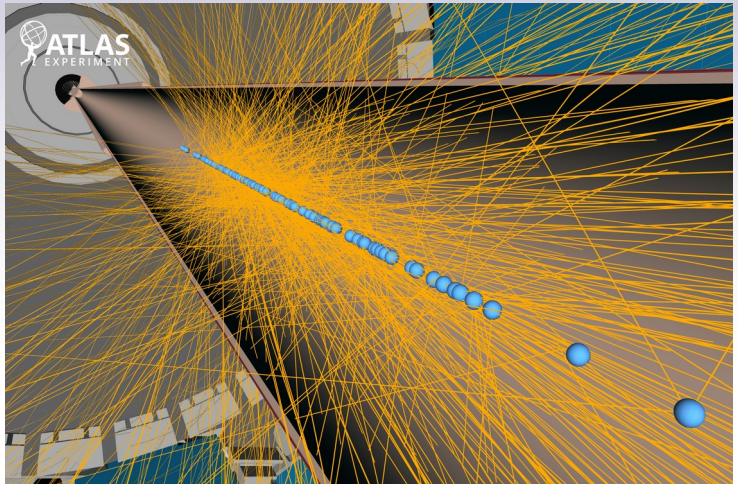


Figure 2: Proton-proton Collisions.

Current Luminosity:

$$\mathcal{L} \simeq 2 \times 10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$$

Luminosity to reach:

$$\mathcal{L} \simeq 7.5 \times 10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$$

[1] V. Raskina, S. Trincaz-Duvoid, T, Beau. (2023). Research and development of the High-Granularity Timing Detector (HGTD) for the ATLAS Detector as the preparation of the High-Luminosity LHC operation phase. LPNHE, France. Recovered from: https://cernbox.cern.ch/s/z2sc5NLgnVpBPOp

Introduction: ATLAS and HGTD

-HGDT offers a new and powerful technique to overcome the pile-up obstacle by taking advantage of the temporal dispersion of interactions [2].

$$\eta = -\ln\left[\tan\left(\frac{\theta}{2}\right)\right]$$

-This detector will be built using LGAD sensors. The HGTD can also be used as a luminosity measurement device [2].

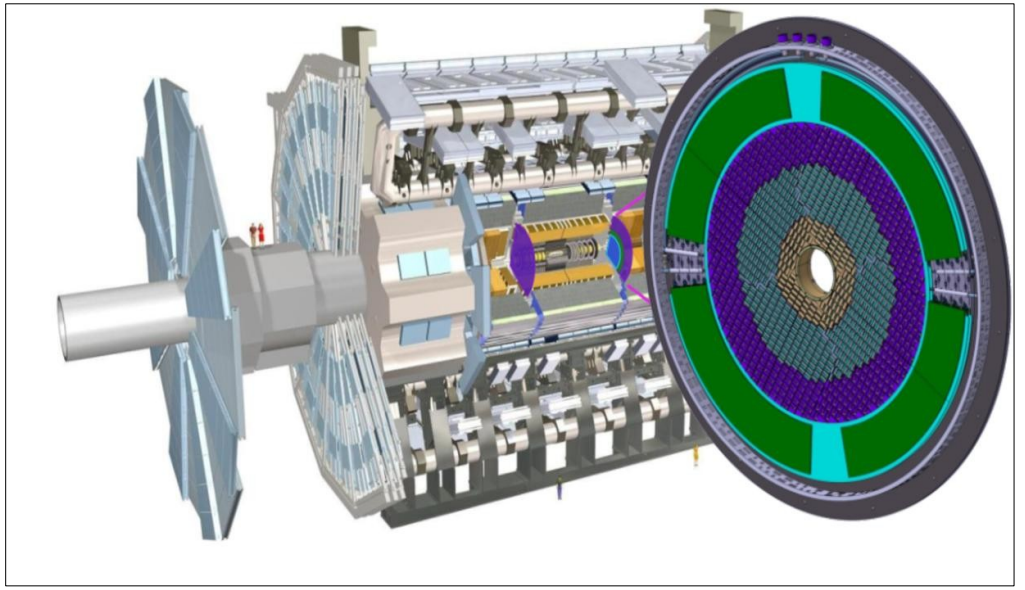


Figure 3: HGTD inserted in ATLAS.

Region to be covered:

$2.4 < \eta < 4.0$

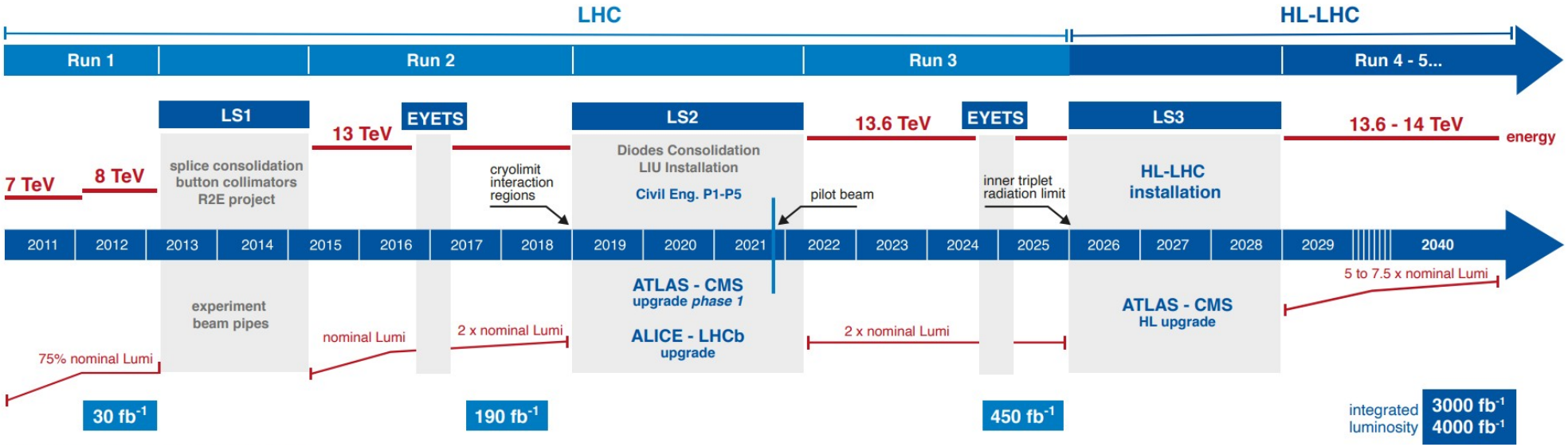
Time resolution: 30-50 ps.

LA-CoNGA physics [2] *A High-Granularity Timing Detector in ATLAS : Performance at the HL-LHC.* Corentin Allaire on behalf of the ATLAS LAr-HGTD group LAL, Univ. Paris-Sud, CNRS/IN2P3, Universit Paris-Saclay, Orsay, France.

Experimental Framework: The High Luminosity LHC

From 2026, LHC will be upgraded and in 2029, LHC will run in “High Luminosity" (HL-LHC).

- Increase the number of collisions per unit of time.
- Instantaneous luminosity will be approximately a factor of **~5-7.5** higher than the LHC nominal values.
- Average number of interactions per bunch crossing (pileup events) reaches **200**.
- HL-LHC promises to provide 15 times the present data sample.
- Harsh radiation environment up to 2 x 10^{15} n_{eq} cm^{-2}.
- ATLAS experiment also needs to be upgraded to meet the new requirements.



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Experimental Framework: The High Luminosity LHC

The Pile-up will be caused by the increase of the instantaneous luminosity.

- Pile-up <μ> = 200 interactions per bunch crossing, spread in **~45 mm** along the beam axis [3].
- **The Inner Tracker (ITk)** mostly mitigates the pile-up effect but is still challenging in the forward region [3].
- To discriminate between pile-up and hard scattering interaction, the HGTD will be added in the forward region with the goal to have **30-50 ps** per track time resolution (beginning-end) [3].
- By utilizing both spatial and timing information, we can confidently link tracks to vertices in the forward region [4].

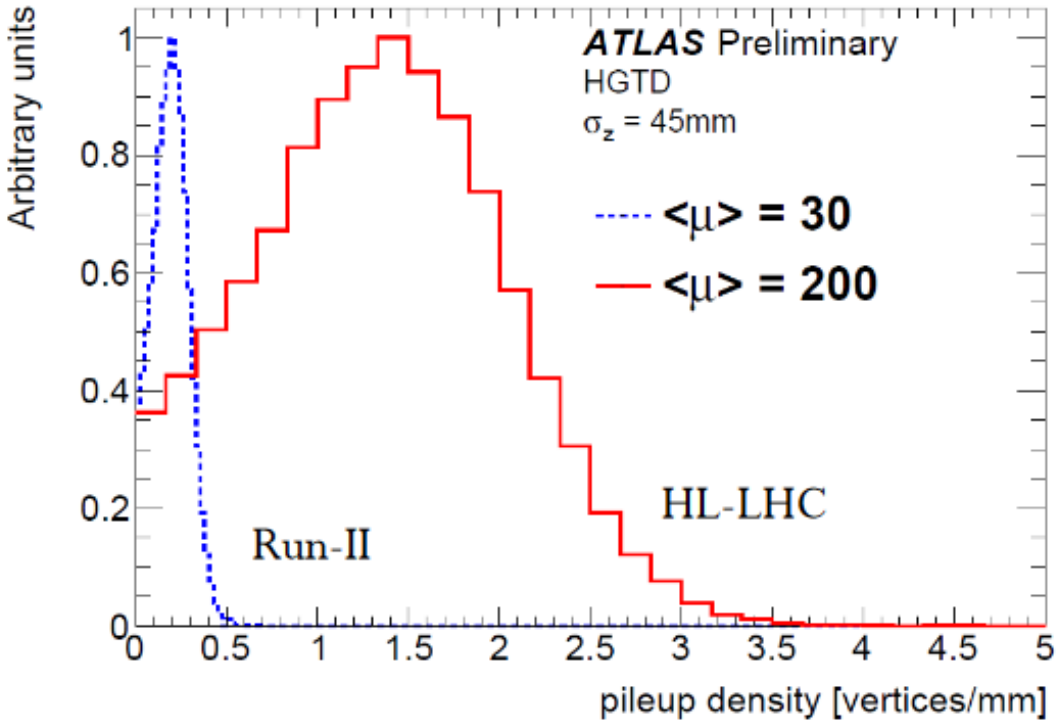

Figure 4: Pile-up differences.

LA-CoNGA physics [3] *Simulation of the ATLAS High Granularity Timing Detector geometry in the ATLAS framework.* Hanane Riani on behalf of the ATLAS HGTD Group (2023). University Mohamed First Oujda. Rabat, Morocco.
[4] *DAQ Activities of HGTD*. Yassine Bimgdi, on behalf of the ATLAS HGTD Group (2023). Mohammed VI Polytechnic University. Ben Guerir, Morocco.
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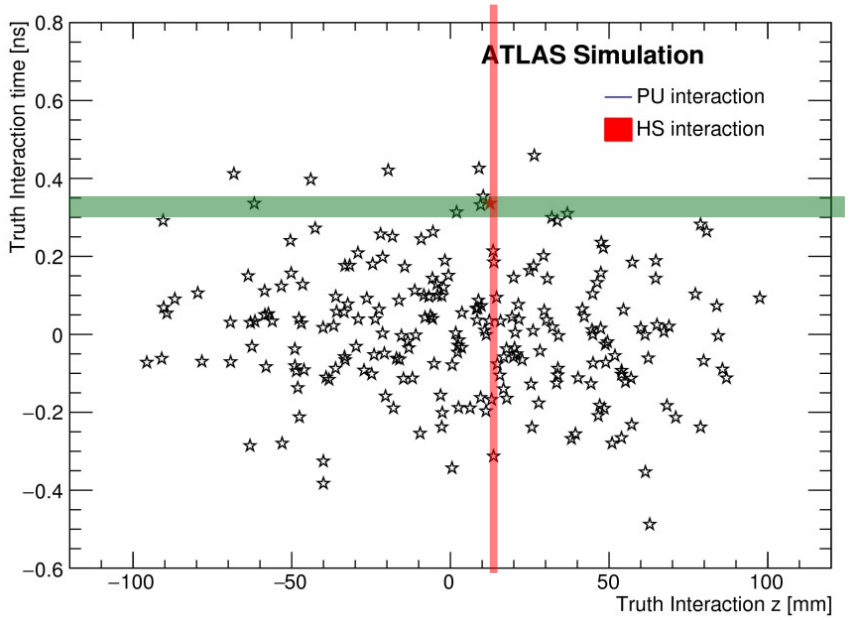
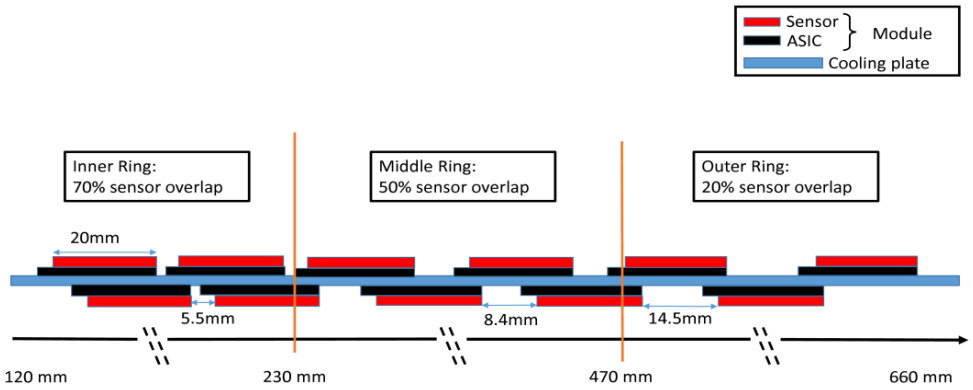
Experimental Framework: The High Granularity Timing Detector (HGTD)

HGTD is proposed in front of the Liquid Argon end-cap calorimeters to reduce pile-up.

- Two instrumented double-sided layers mounted in two cooling/support disks per end-cap [1].
- Placed at **z ≈ ±3.5 m** from the nominal interaction point.
- Total radius **110 < r < 1000 mm** [1].
- Active detector region: **2.4 < |η|< 4, 120 mm < r < 640 mm.**
- Structure is divided into 3 rings with different active sensor overlap (70%, 50%, 20%) [1].
- Time resolution < 30-50 ps per track (start-finish).





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Experimental Framework: HGTD - Geometry Description

Simulation results show good object reconstruction and physics performance by adding HGTD to ITk. HGTD end-caps are instrumented of two double-sided disk.

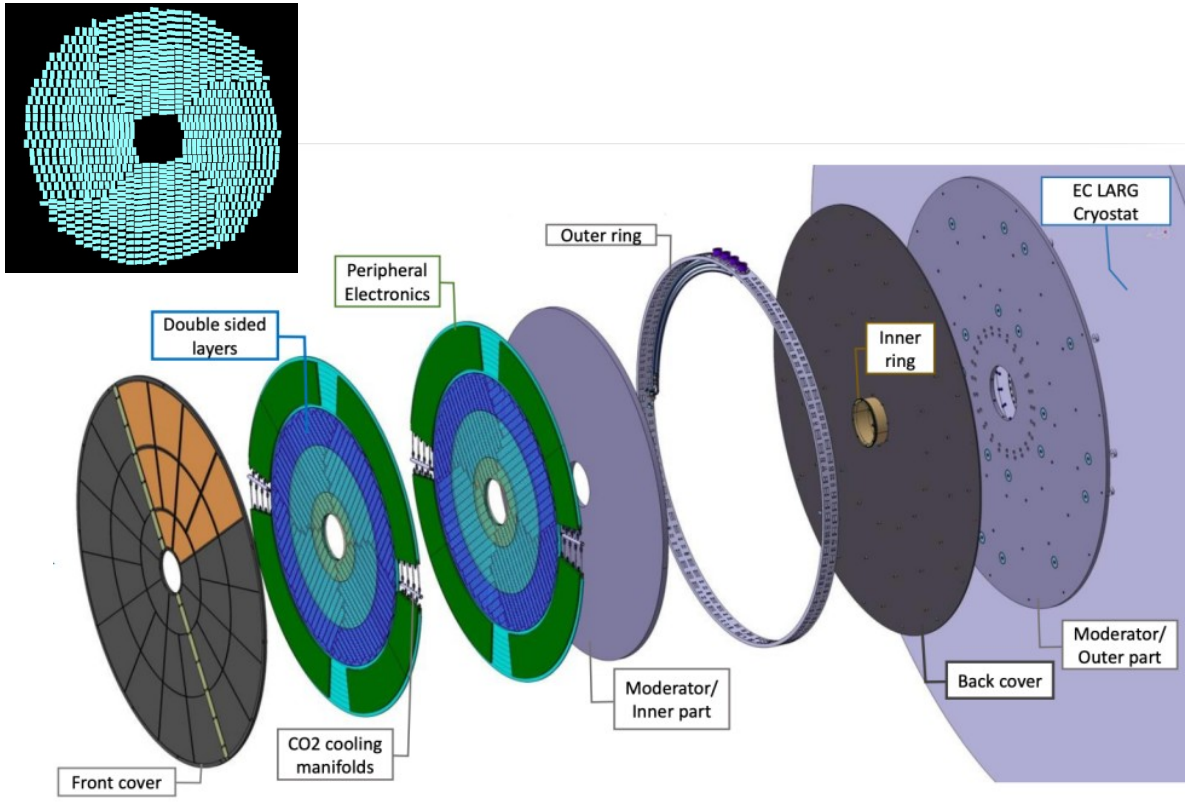

Figure 4: HGTD Geometry

- HGTD disk ➔ 2 module layer + Flex + 2 support plate + 1 cooling plate + Peripheral electronics [2].
- For the flex cables, 8 slices are stacked together, with R_{min} increasing from one to another, resulting in their total thickness decreasing as a function of the radius.
- The peripheral electronics including electronics components such as LGAD, Peripheral electronics, cooling loop prototypes, modules, flex cables, etc [3].

LA-CoNGA physics [2] *A High-Granularity Timing Detector in ATLAS : Performance at the HL-LHC.* Corentin Allaire on behalf of the ATLAS LAr-HGTD group LAL, Univ. Paris-Sud, CNRS/IN2P3, Universit Paris-Saclay, Orsay, France.
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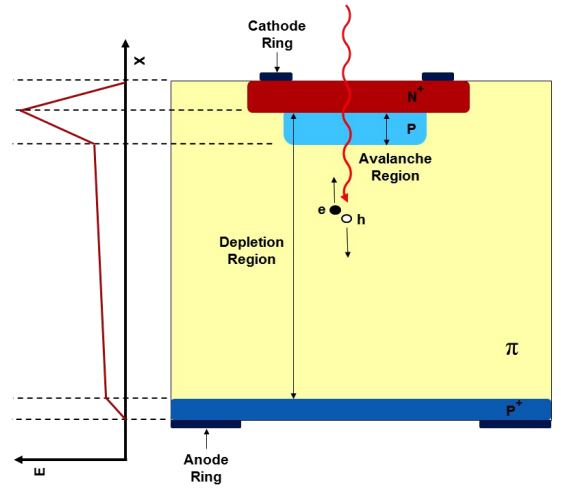
Experimental Framework: The LGAD sensors for the HGTD

LGAD is a new silicon detector technology developed recently, that could measure the particle time at ps precision.

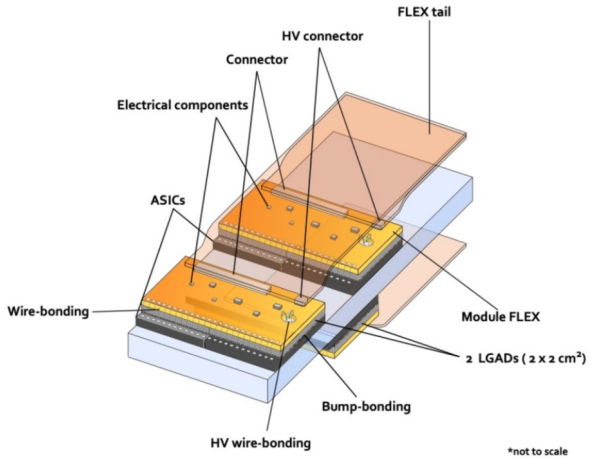
A good time resolution of HGTD will be achieved by using the Low Gain Avalanche Detectors (LGAD), the new semiconductor sensors technology meant for precise timing measurements [2].

Although a track may appear to align spatially with a particular vertex, differences in the track's time and the selected vertex's time can be used to identify and discard pile-up tracks [2].



Sensor technology: Low Detector (LGAD)

- **n-p Si** detector with an additional p-type doped layer.
- Excellent time resolution **< 30 ps** pre-irradiation [3].
- Fast rise time **~ 0.5 ns**.
- Hit efficiency **> 95%** at the end of lifetime.
- Several prototypes: CNM (Spain), HPK (Japan), FBK (Italy), IME (China), NDL (China) [3].



Adrián Vásquez

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Experimental Framework: Modules

When a particle passes, it creates charges which are collected forming a signal.

- HGTD has 8032 modules.
- Two 15x15 LGAD sensors bump-bounded to two ASICs (15x15) with pads of 1.3x1.3 mm^2.
- 3.6 M channels operating at -30°C.
- 2 x 4 cm^2 dimensions.
- Modules mounted on the cooling plate, connected to the surrounded Peripheral Electronics Board (PEBs) via FLEX tail cable.
- LGAD is connected to ALTIROC through Bump Bonding.

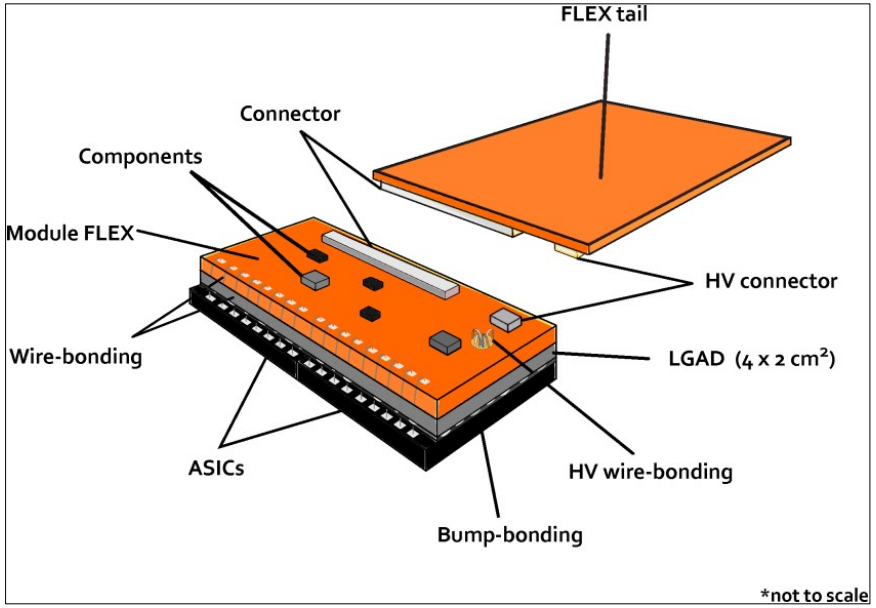
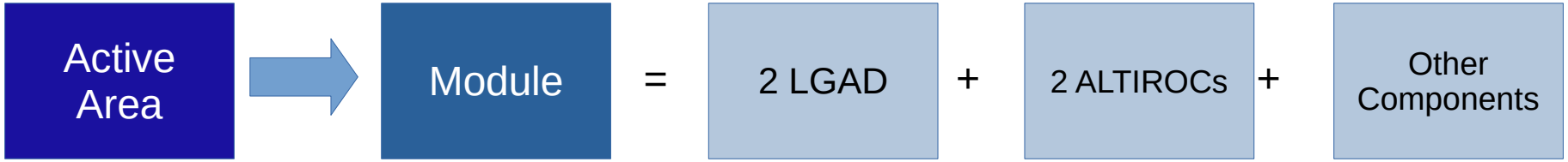


Figure 5: Diagram of a Module



[3] *Simulation of the ATLAS High Granularity Timing Detector geometry in the ATLAS framework.* Hanane Riani on behalf of the ATLAS HGTD Group (2023). University Mohamed First Oujda. Rabat, Morocco.

Methodological Framework: Activity Scheme

General Objective:

Develop the routines (both instrumental and computational) for the electronic testing processes, taking and analyzing the results of the modules for the FM01DU Detector Unit of the HGTD, in the LPNHE facilities of the Sorbonne Université/Université Paris Cité.

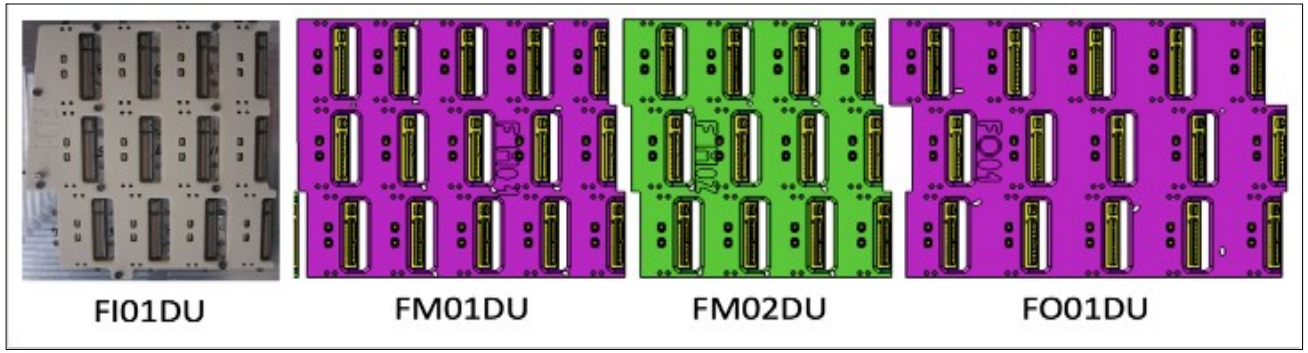


Figure 6: Diagram of the Demonstrator at LPNHE (DU of HGTD).

Activities:

- Carrying out electronic tests (along with their analysis) on the modules to be used in the FM01SU detector unit.
- Preparation of codes in bash, python and Gcode for the automation of tests as well as updating the codes for the “Gluing” activities.

Methodological Framework: Instruments and Tests done

Instruments:

- Aim TTI DC PSU QL3564.
- Aim TTI DC PSU PLH120.
- CAEN HV Power Supply DT803x.
- ALTIROC Low Gain Avalanche Detector (LGAD) Modules.
- Flex PCB tail for Module and microcontroller board connection.
- FPGA Model Microcontroller Board.
- FADA software for carrying out Tests and Analysis.

Tests Done:

- Bump Connectivity test: HV Off.
- Bump Connectivity test: HV On.
- Tunning Module test: Threshold Scan.
- Tunning Module test: VTHC Scan.
- Tunning Module test: Charge Scan.

List of Modules in LPNHE:

- FBM-FR-012-LEO
- FBM-FR-016-PRI
- FBM-FR-021-UGO
- FBM-FR-022-VIN
- FBM-FR-023-WAN
- FBM-FR-025-YMI
- FBM-FR-027-AFR
- FFM-FR-028-BOS

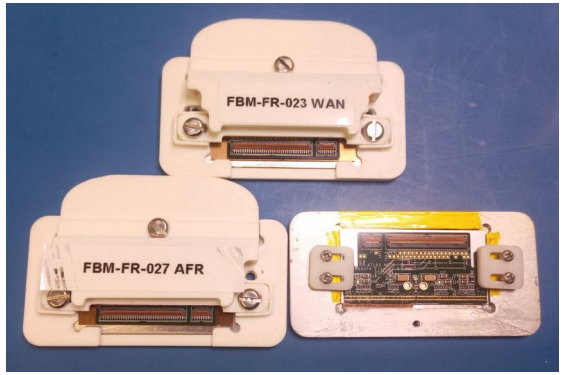


Figure 7: Examples of modules.

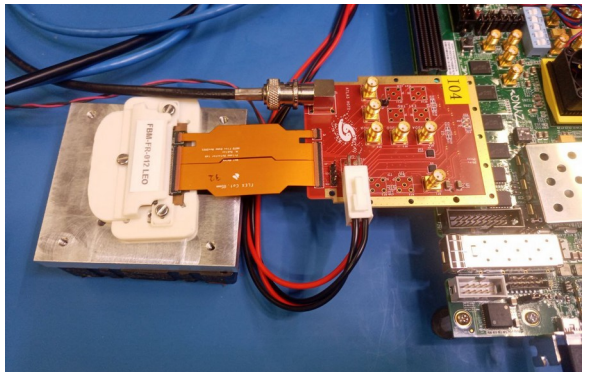


Figure 8: Module connected to board

Methodological Framework: Experimental Setup

1. Design and elaboration of the commands and bash codes for the tests.

2. Connection of the modules and Power Supplies to the board card.

3. Realization of bump Connectivity test with HV Power supply Off.

4. Connection of HV Power Supply to the circuit.

5. Realization of bump Connectivity test with HV Power supply On.

6. Realization of Tunning Module tests (with HV Power supply On).

Figure 9: Experimental Setup in the lab.

Repeat from the step 2. to step 6. for the rest of the modules.

Results and Analysis: Code for tests

The code produce in the lab for test use FADA (Framework for Altiroc Data Acquisition) and was written in bash.

FADA is a project is divided in two main repositories. The first one contains the ***firmware*** (including also the server). The second one contains the ***software*** written in python and the instructions for the installation and to perform various measurements.

The routines in the code can be used to:

- Check bump connectivity in the modules (connection between sensors and chips)
- Turn the Power supplies on and off by the use of Socket Python library.
- Show graphs of how noisy the Pixels in the module could be.

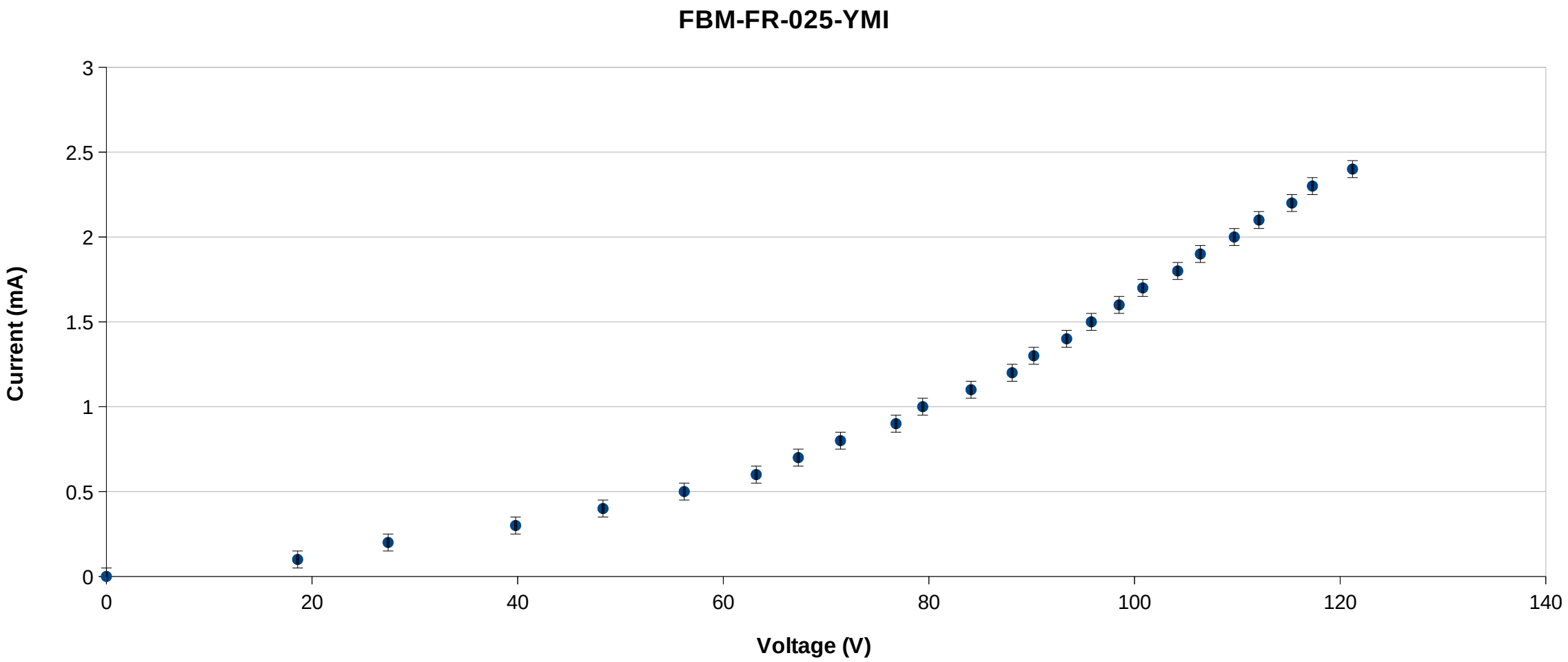
```
  python3 -c "import socket; import socketscpi as scpi; supply1 =
scpi.SocketInstrument('$Inst1', $PORT, verboseErrCheck=True); supply2 =
scpi.SocketInstrument('$Inst2', $PORT, verboseErrCheck=True);
supply1.write('OPALL 1'); supply2.write('OPALL 1')"
}

Bump_Connection () {
  cd
  more Downloads/Modules_list.txt
  read -p "Introduce the number of your module:" j
  P=$(echo "$(awk "{if(NR==$j) print $2}" Downloads/Modules_list.txt)" |
cut -c3-)
  yourMeasurementName=${P}${now}
  yourMeasurementOld="$P"
  echo $yourMeasurementName
  bump='bump'
  bumpname="${bump}_${yourMeasurementName}"
  echo $bumpname
  sshpass -p $SD ssh -t user@$m "cd ~/FADA/firmware/FastFADA2ASIC;
                                 source check_bump_connection_manual.sh
$bumpname $Pow"
  mkdir -p $Measurement_Path/"$yourMeasurementName"/bumpConnection
  cd FADA/software/analysis/FastFadaAnalysis
  python3 makeEffCurve.py --module --input $home/$Measurement_Path/
Measurements2ASIC/bump_"$yourMeasurementName"_Hv$Pow1/thresScan/
B_22_On_col_Inj_col_N_20_Q_38/ --prefix HV_"$Pow1"_Q_38 --output-dir
$home/$Measurement_Path/"$yourMeasurementName"/bumpConnection
  cd
}

Tuning_Module () {
  cd
  more Downloads/Modules_list.txt
  read -p "Introduce the number of your module:" j
  P=$(echo "$(awk "{if(NR==$j) print $2}" Downloads/Modules_list.txt)" |
cut -c3-)
  tunning='TM_'
  HvPow='_Hv'
  yourMeasurementName=${tunning}${P}${now}
  yourModuleName=$P
  TM_yourModuleName=${tunning}${P}
  echo $yourMeasurementName
```

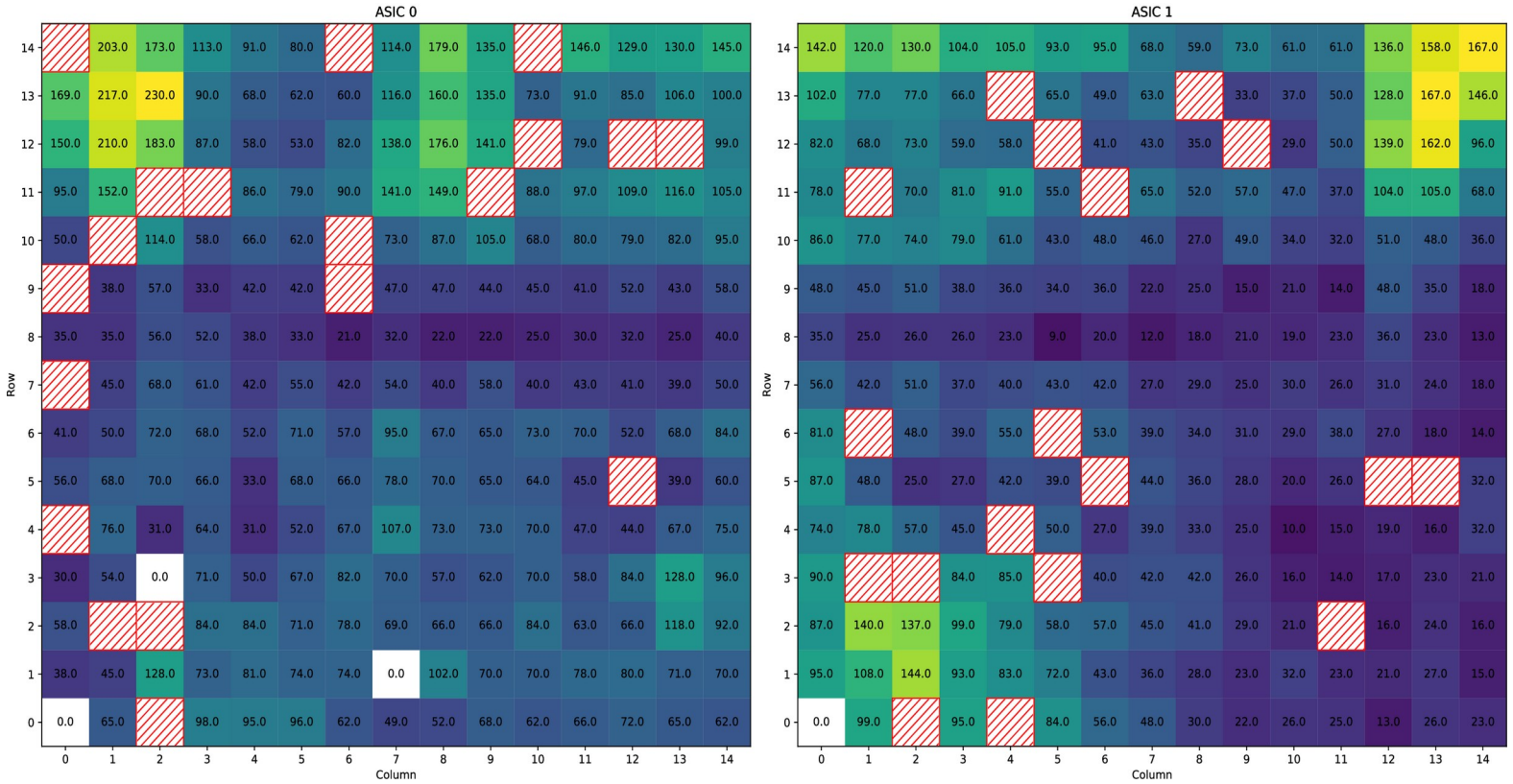
Figure 10: Piece of code with FADA instructions for tests.

Results and Analysis: Module FBM-FR-025 YMI



Results and Analysis: Module FBM-FR-025 YMI

Bump Connectivity test (IJCLAB)



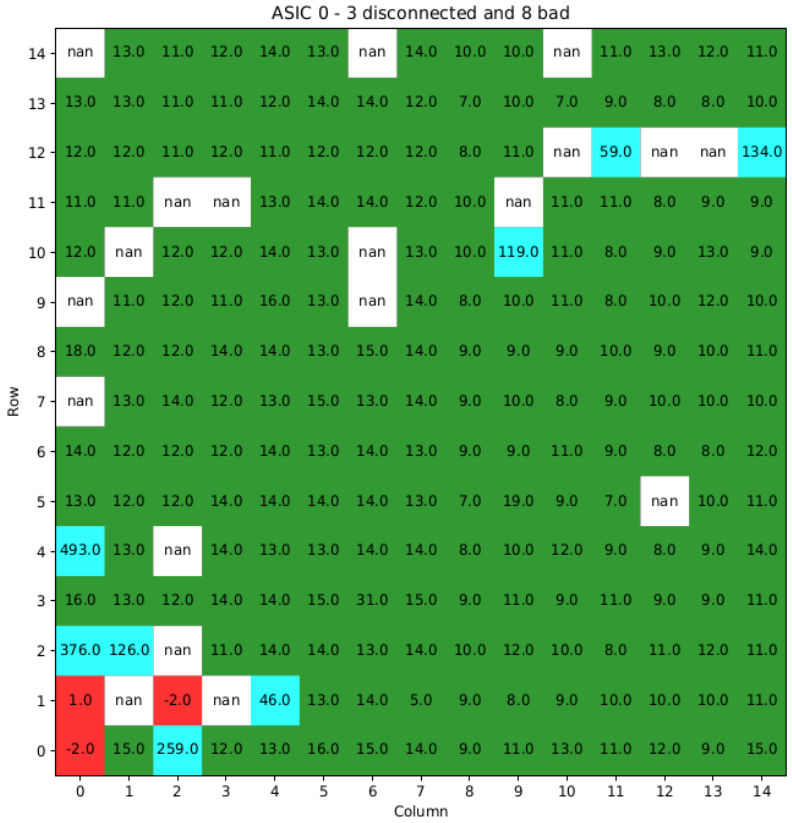
-Test: HV = (120.01 ± 0.01) V ; I = (2.3 ± 0.1) mA

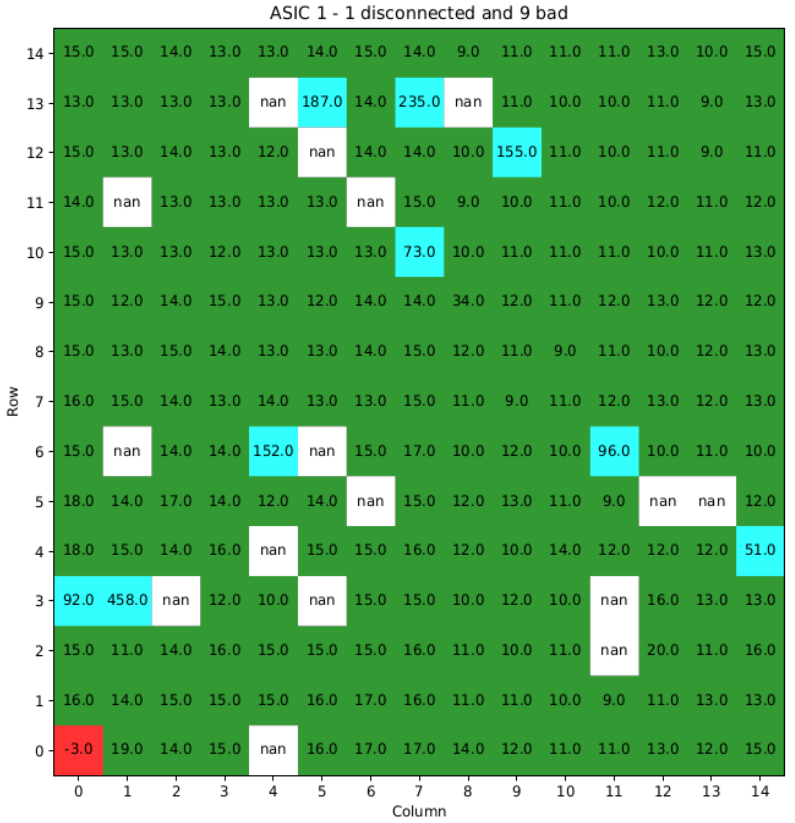
Analysis and comments:

- This test was done with a nuclear β-decay source.
- This is done inmediatly after module assambly at IJCLab
- This shows some pixels are very noisy but just three are disconnected.

Results and Analysis: Module FBM-FR-025 YMI

Bump Connectivity test (LPNHE)



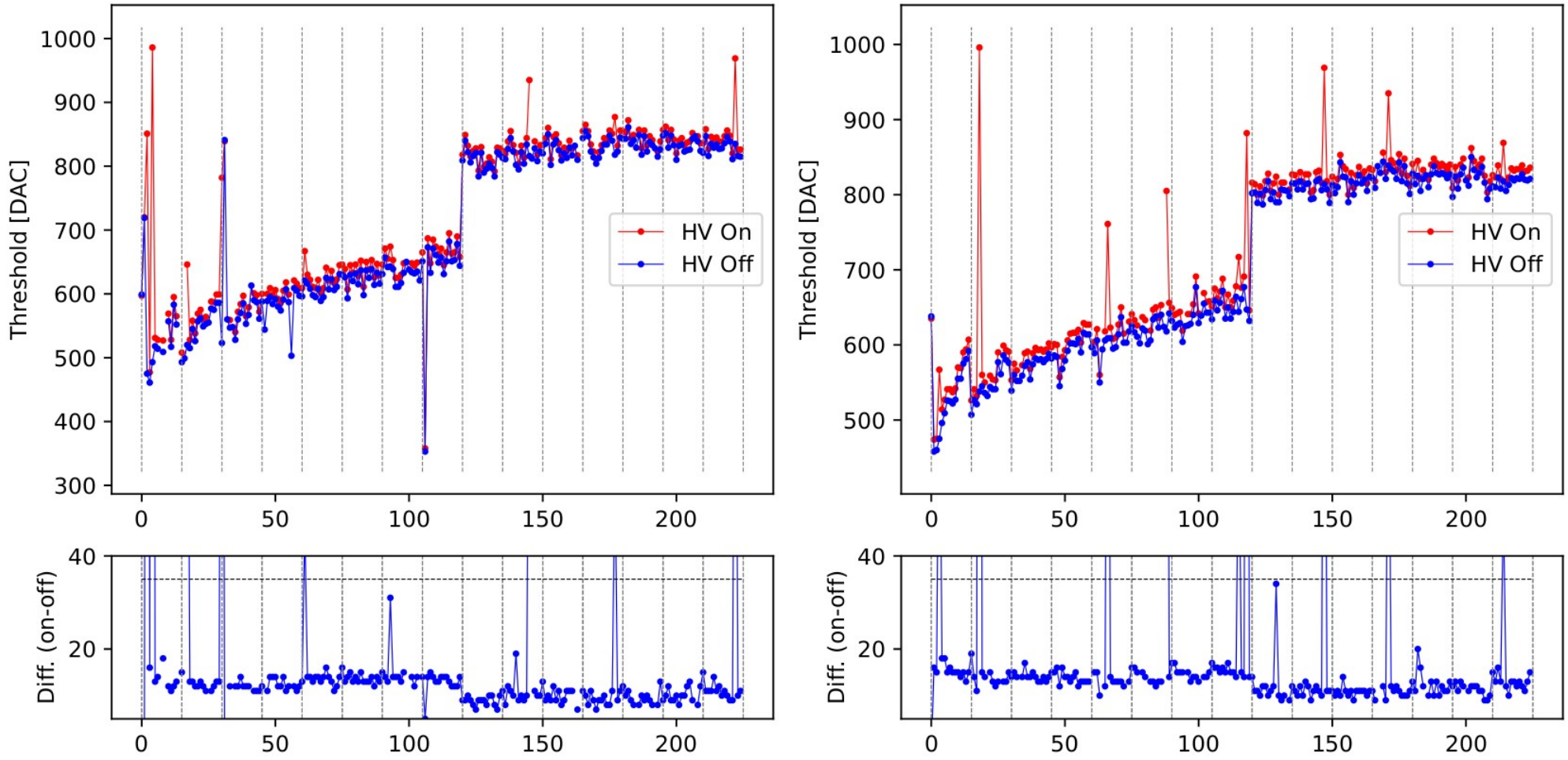


-Test: HV = (120.04 ± 0.01) V ; I = (2.3 ± 0.1) mA

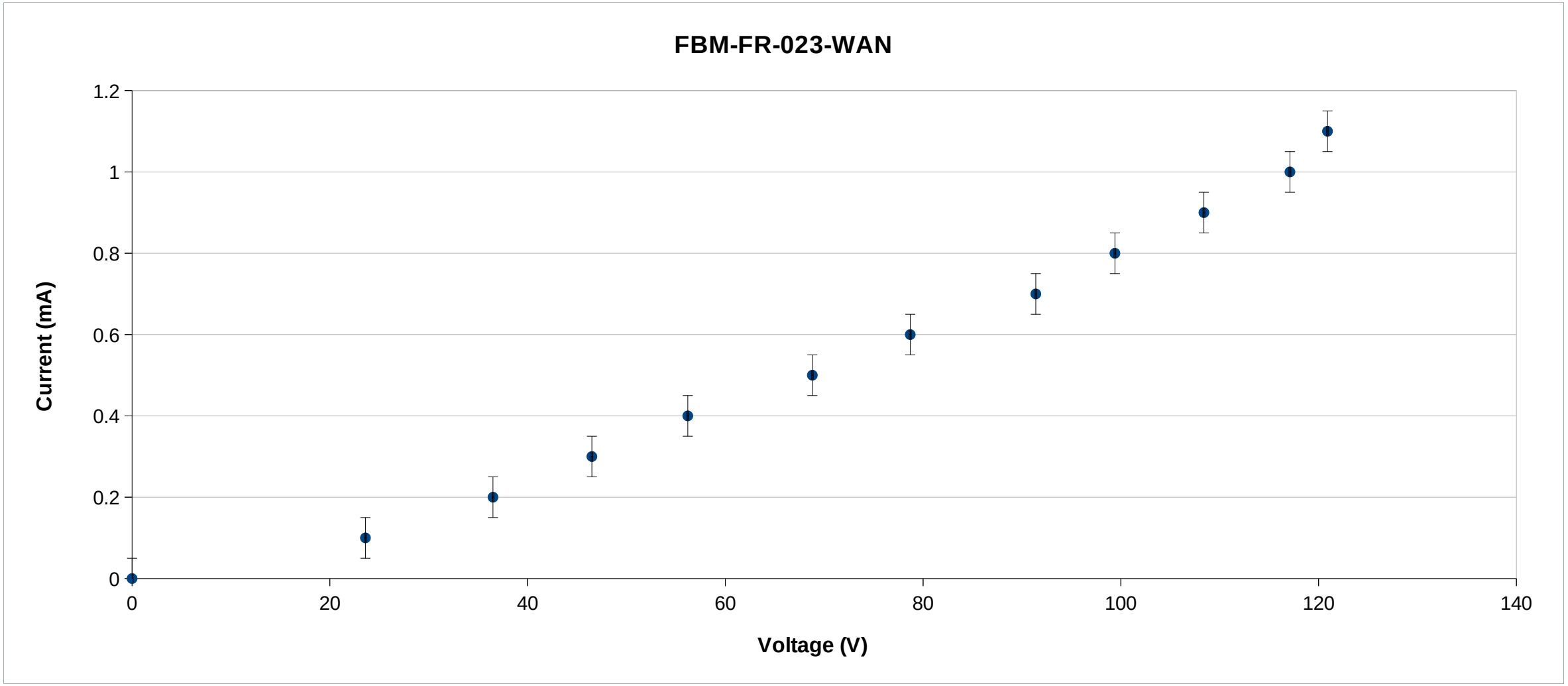
Analysis and comments:

- Test done before loading at DU at LPNHE.
- Difference of the level of noise with HV off and HV on.
- There is a similarity in the location of noisy pixels with IJCLab test.
- This can be used in Demonstrator.

Results and Analysis: Module FBM-FR-025 YMI

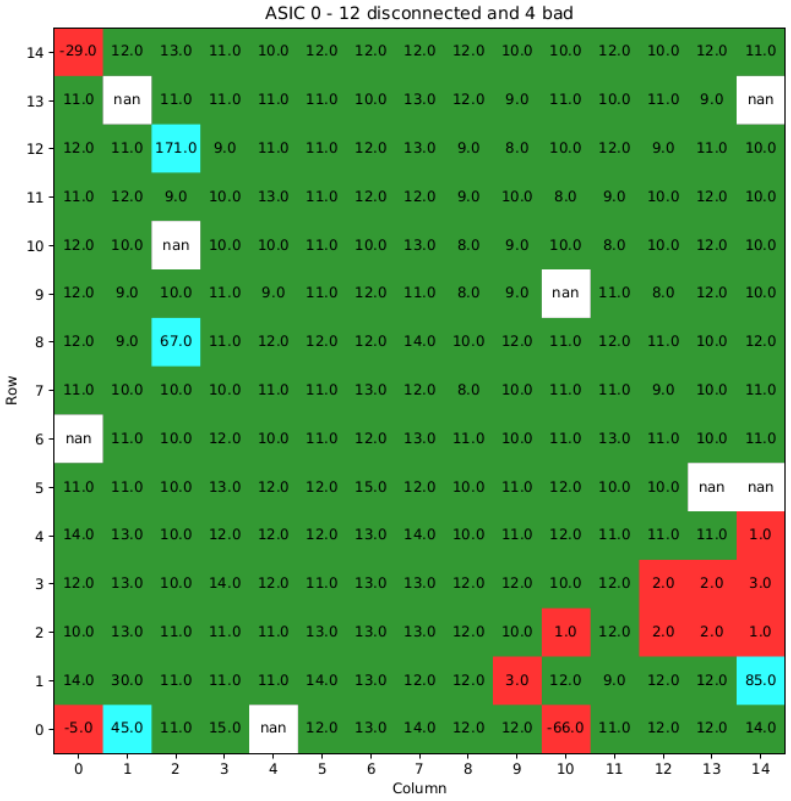


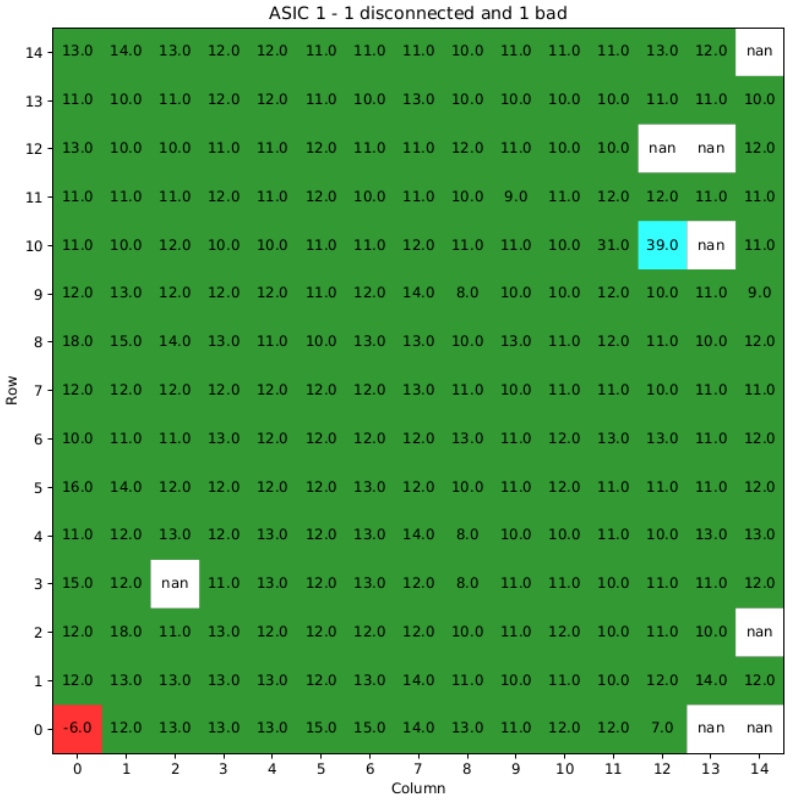
Results and Analysis: Module FBM-FR-023 WAN



Results and Analysis: Module FBM-FR-023 WAN

Bump Connectivity test (LPNHE)



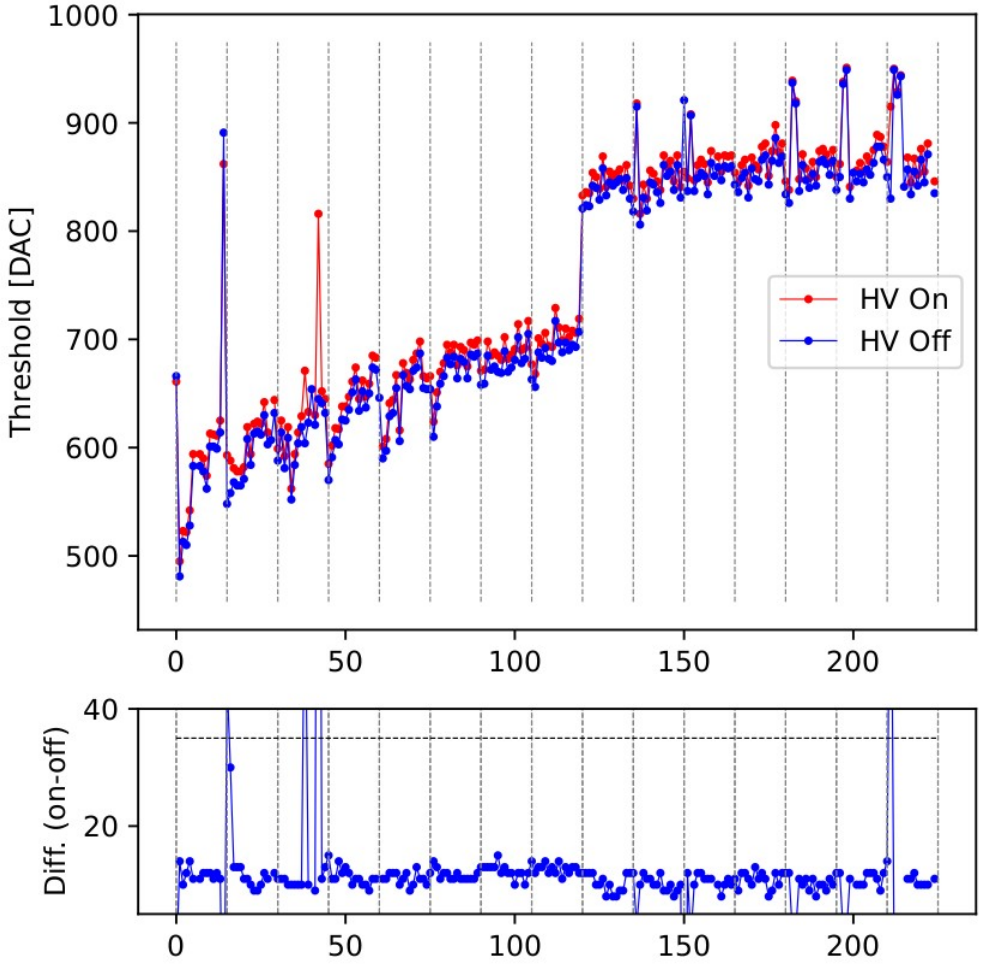


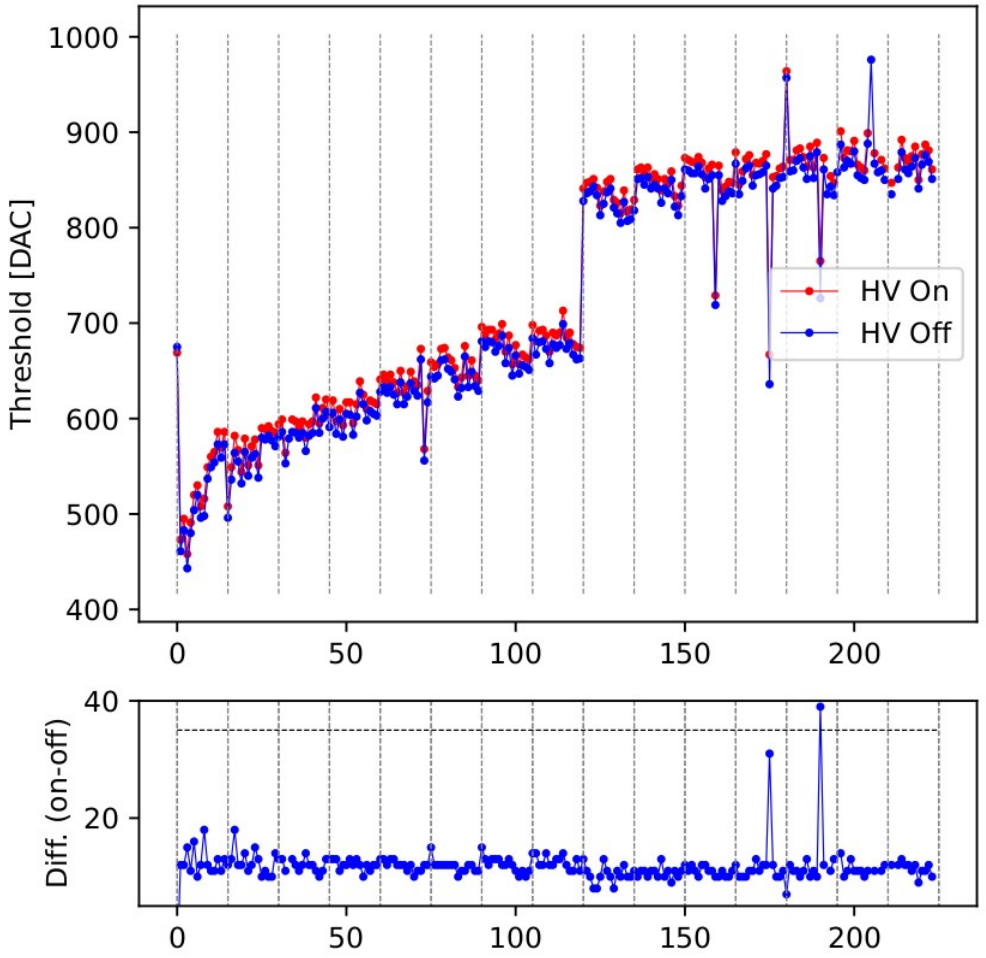
Analysis and comments:

- There's no IJCLab bump Connectivity test for this module.
- Much less noisy pixels than the previous one.
- More disconnected pixels that the previous one.
- This can be used in Demonstrator.

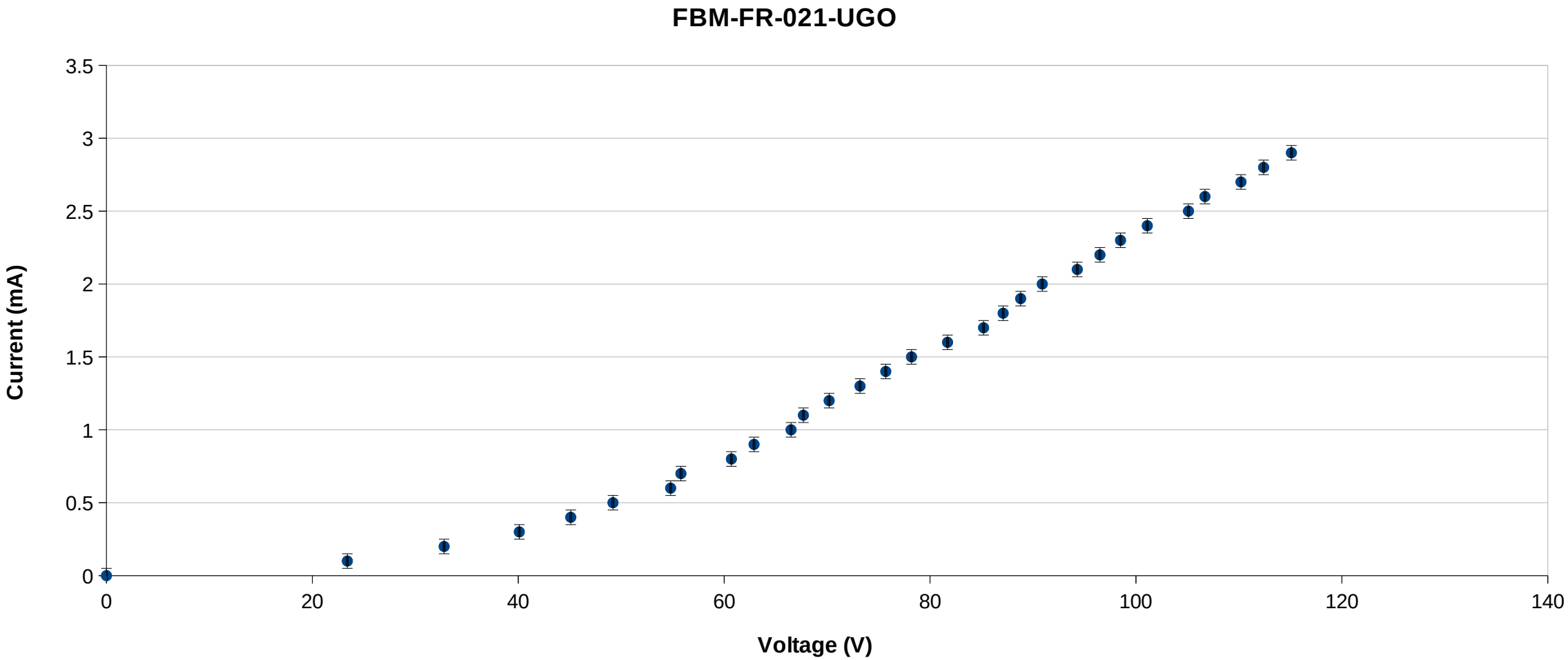
-Test: HV = (120.04 ± 0.01) V ; I = (1.0 ± 0.1) mA

Results and Analysis: Module FBM-FR-023 WAN



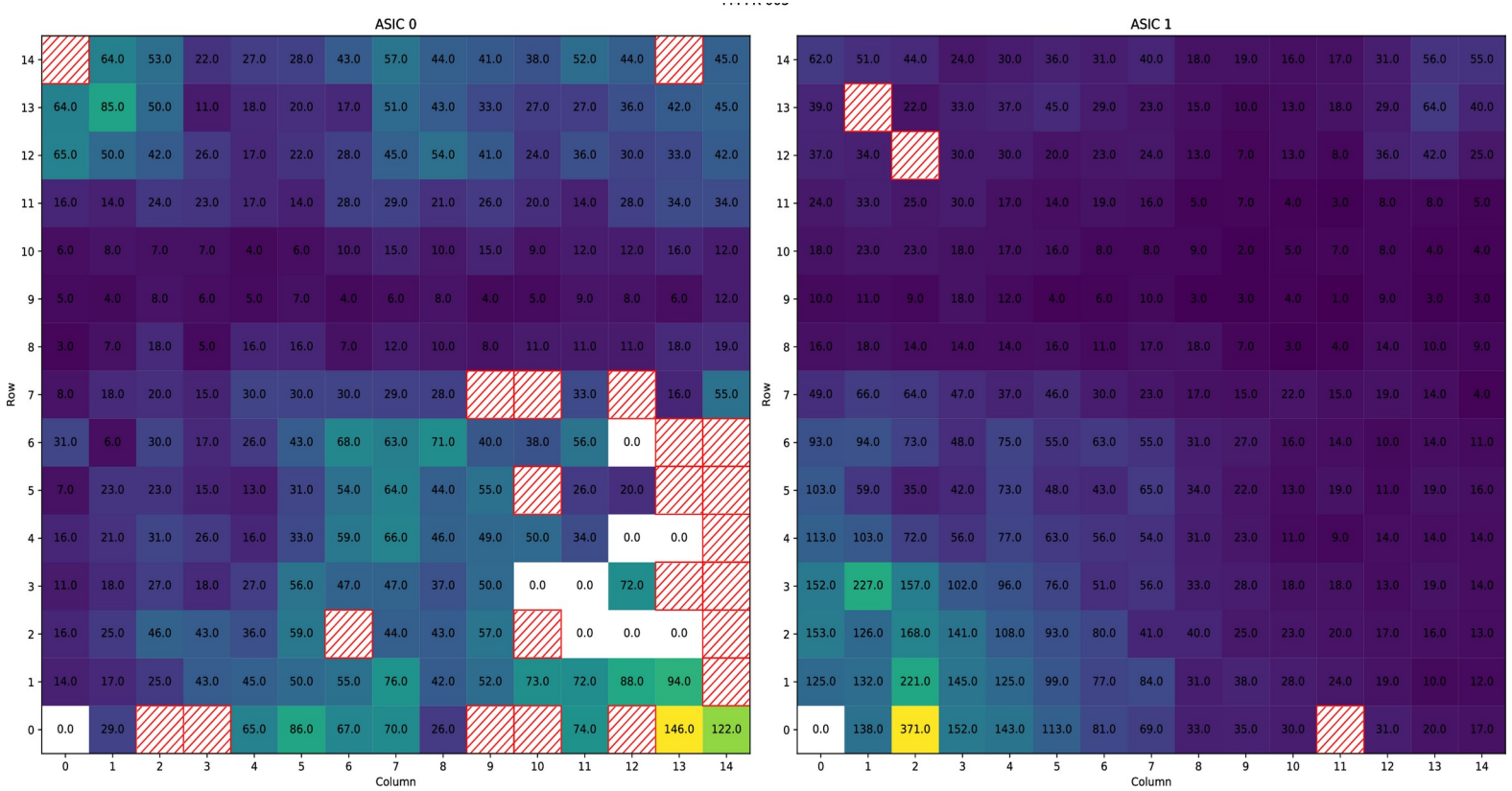


Results and Analysis: Module FBM-FR-021 UGO



Results and Analysis: Module FBM-FR-021 UGO

Bump Connectivity test (IJCLAB)



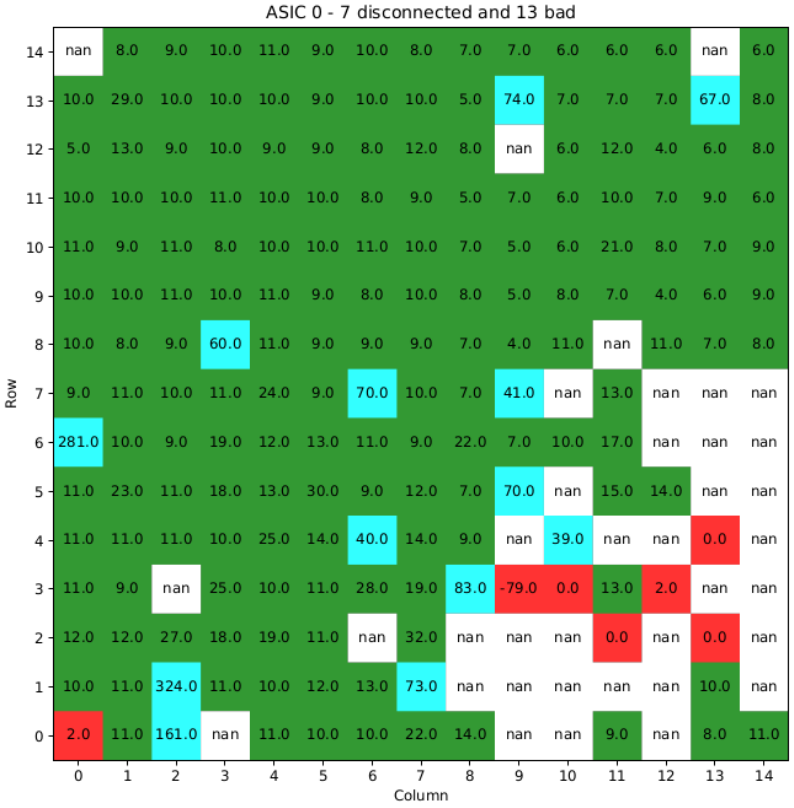
-Test: HV = (100.08 ± 0.01) V ; I = (2.4 ± 0.1) mA

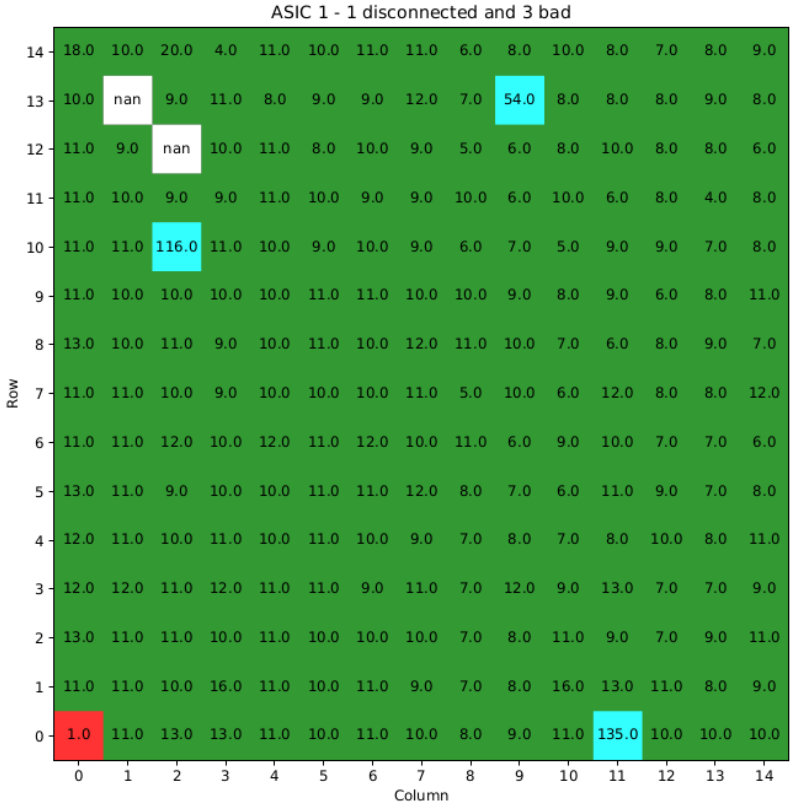
Analysis and comments:

- This test was done with a nuclear β-decay source.
- This is done inmediatly after module assambly at IJCLab
- This shows that Chip 1 (ASIC 1) is in better conditions that Chip 0.

Results and Analysis: Module FBM-FR-021 UGO

Bump Connectivity test (LPNHE)



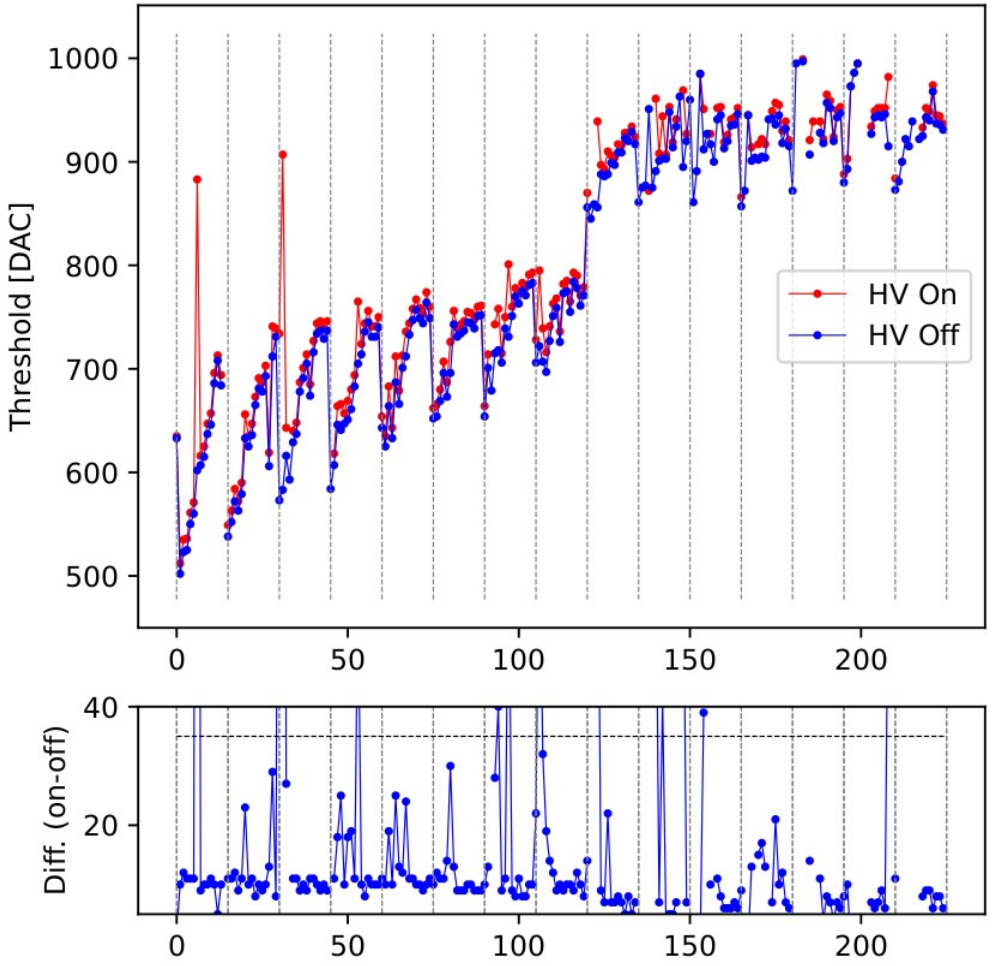


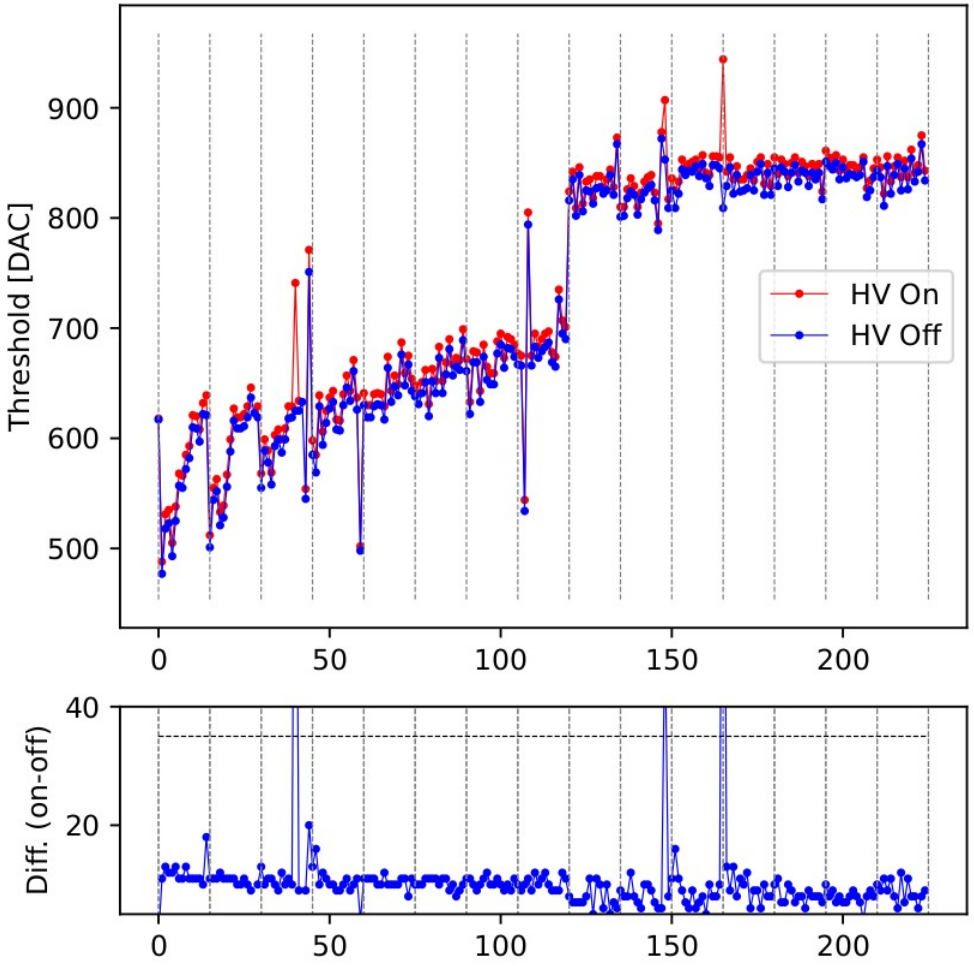
-Test: HV = (100.08 ± 0.01) V ; I = (2.4 ± 0.1) mA

Analysis and comments:

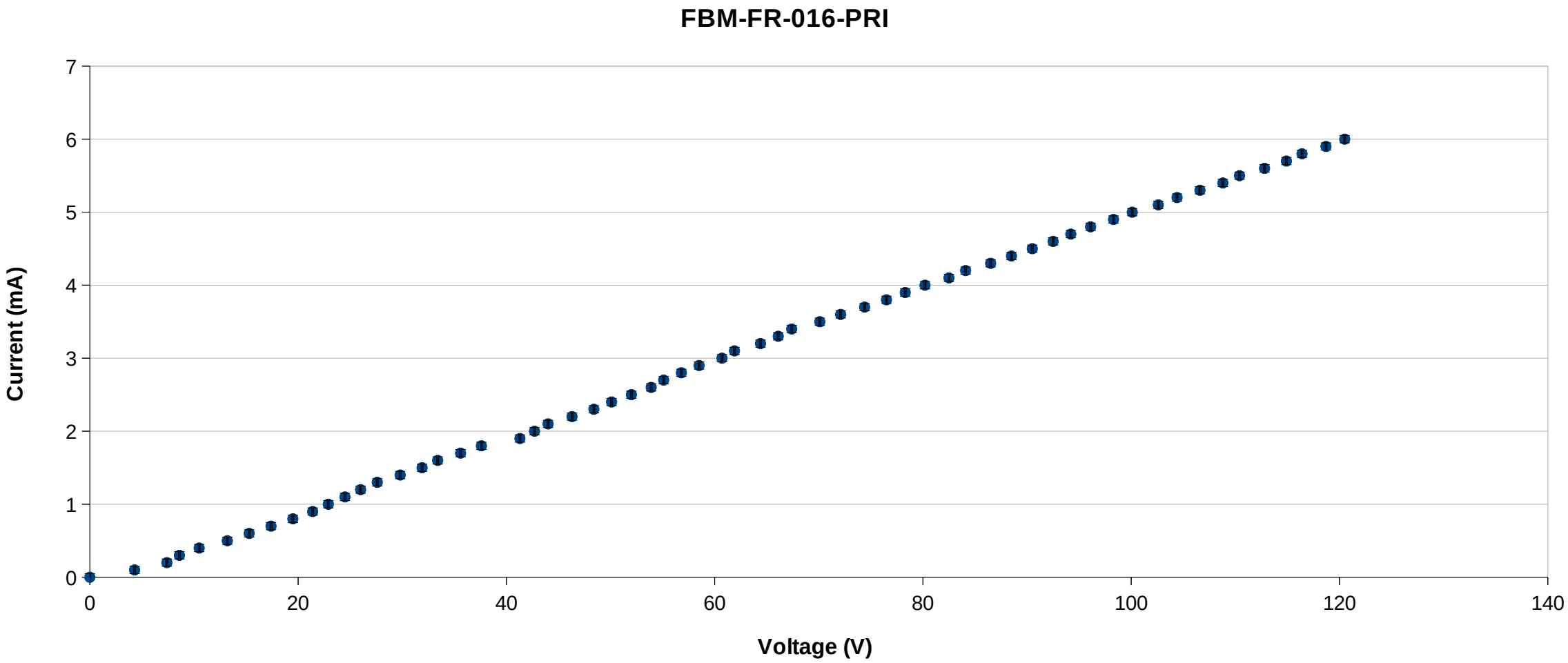
- Test done before loading at DU at LPNHE.
- Difference of the level of noise with HV off and HV on.
- There is a very good similarity with IJCLab test.
- This can be used in Demonstrator.

Results and Analysis: Module FBM-FR-021 UGO



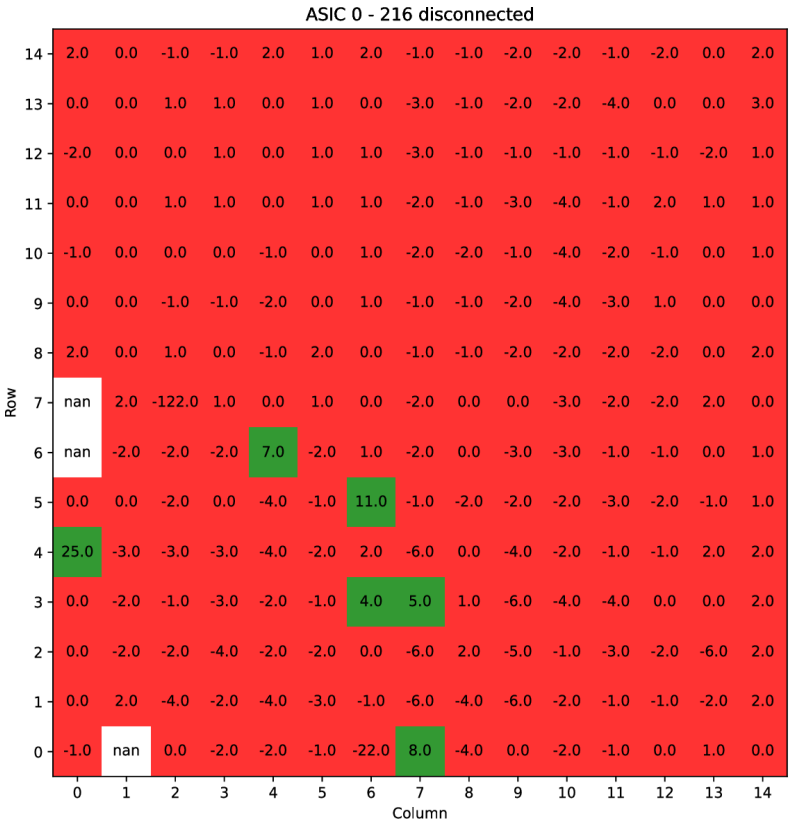


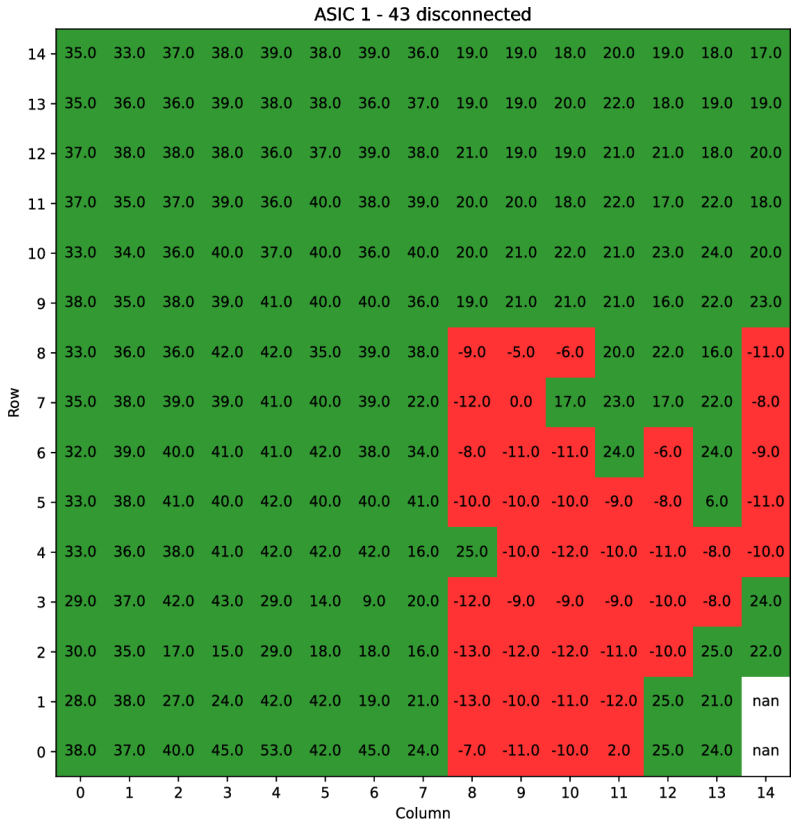
Results and Analysis: Module FBM-FR-016 PRI



Results and Analysis: Module FBM-FR-016 PRI

Bump Connectivity test (IJCLAB)





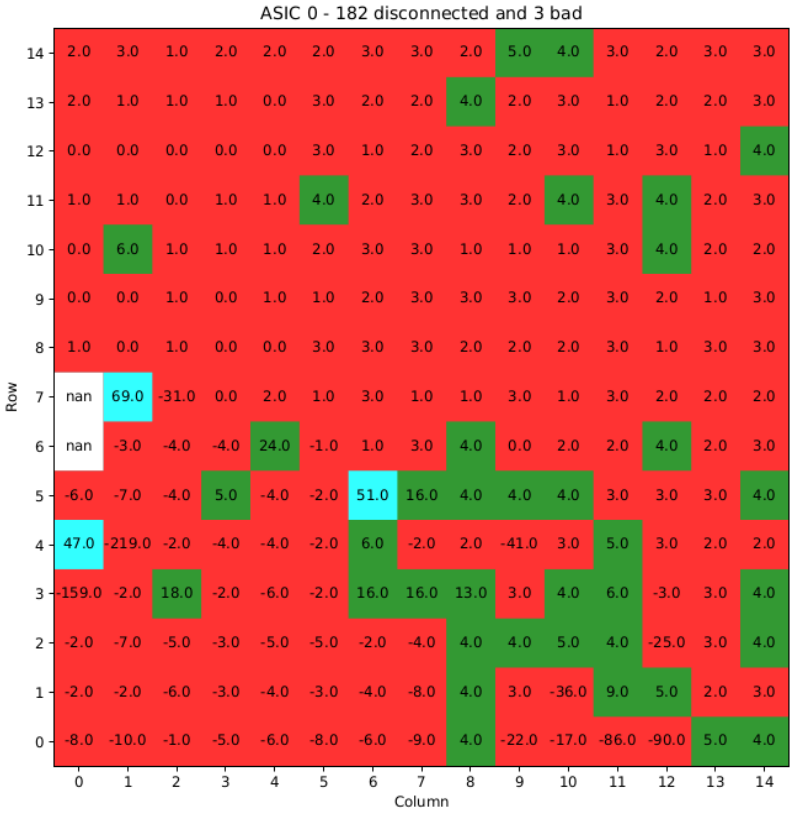
-Test: HV = (120.09 ± 0.01) V ; I = (5.9 ± 0.1) mA

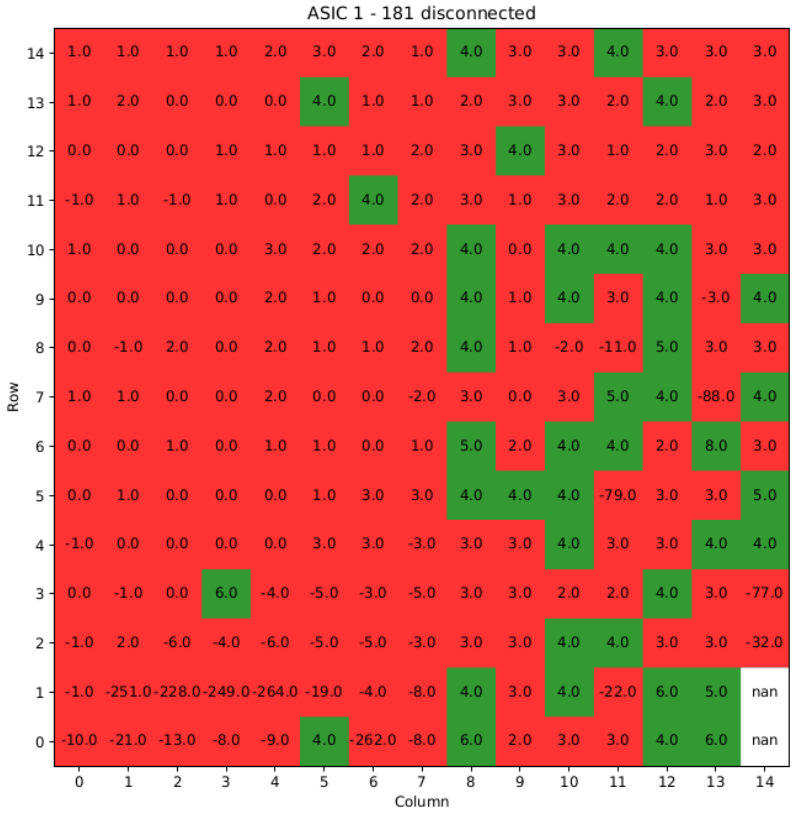
Analysis and comments:

- For this it was performed an electronic bump-connectivity test.
- The Chip zero is not useful (it's almost totally disconnected).
- There is an important quantity of disconnected pixels in chip one.

Results and Analysis: Module FBM-FR-016 PRI

Bump Connectivity test (LPNHE)



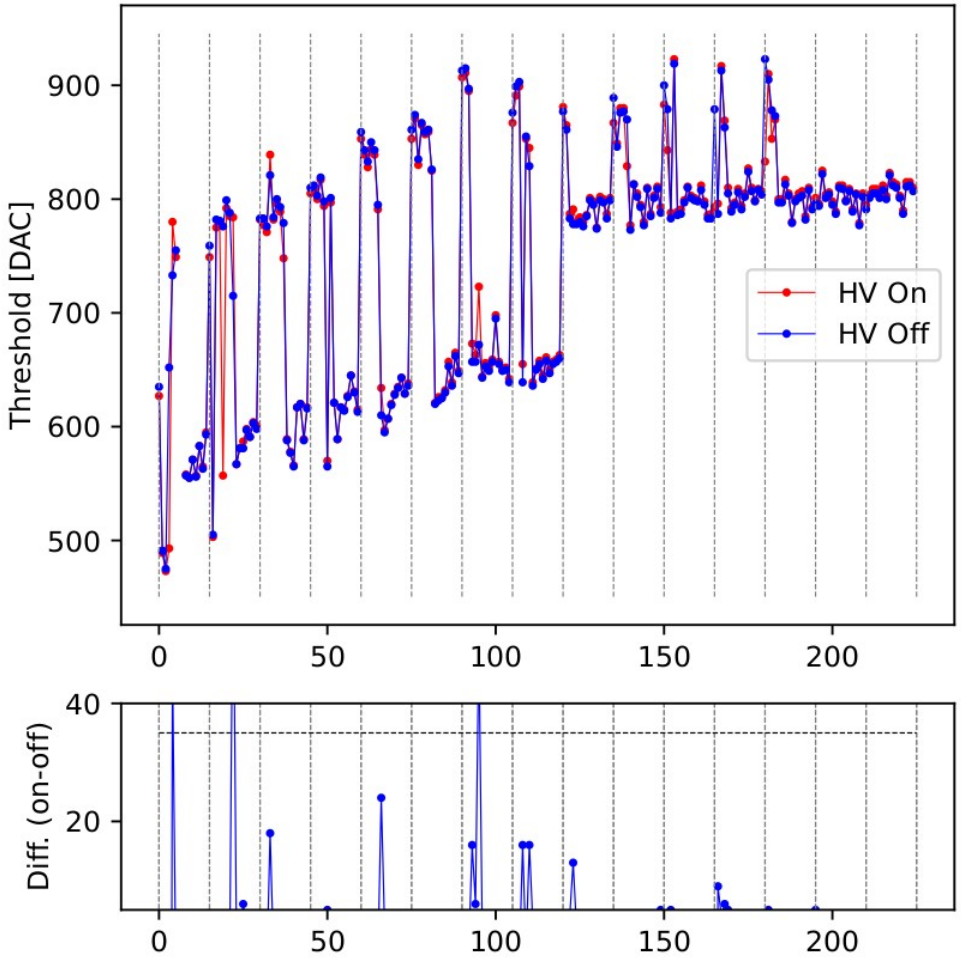


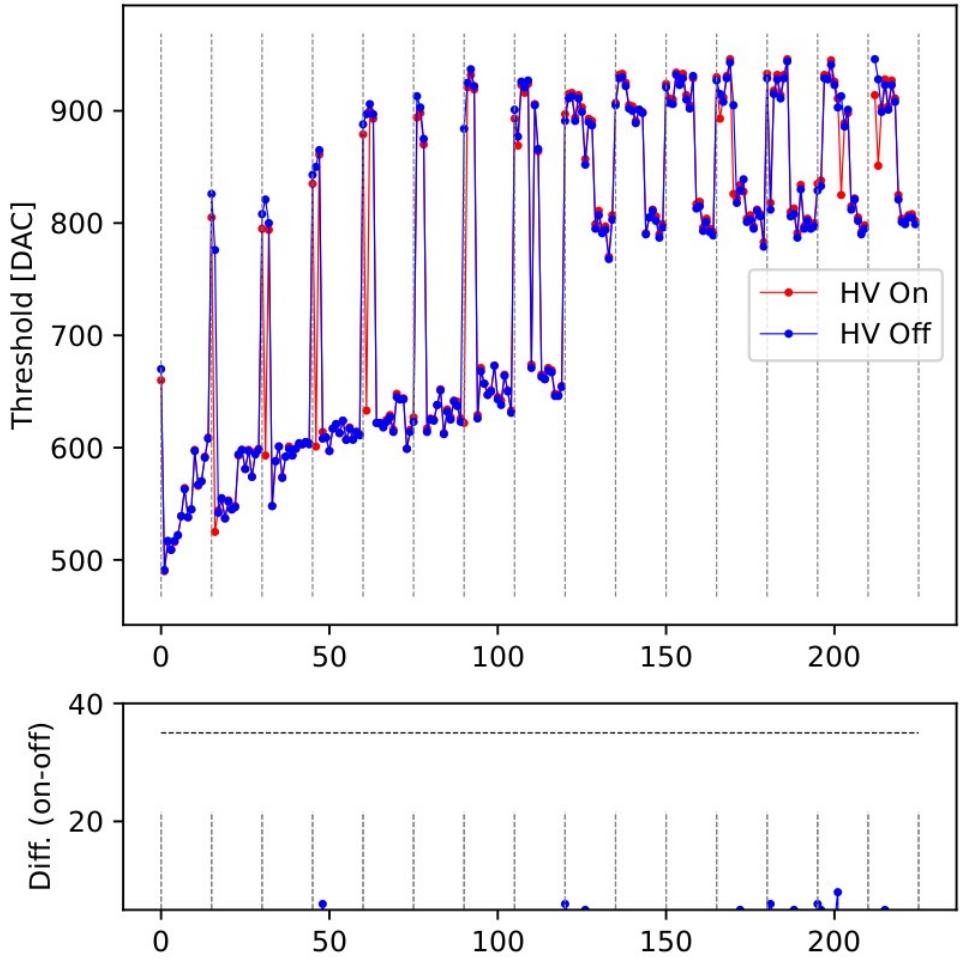
Analysis and comments:

- This module is very damaged.
- The results are very different in comparison with IJCLab.
- The most of the pixels are disconnected in chip one and zero.
- This module will be used just for assembly studies.

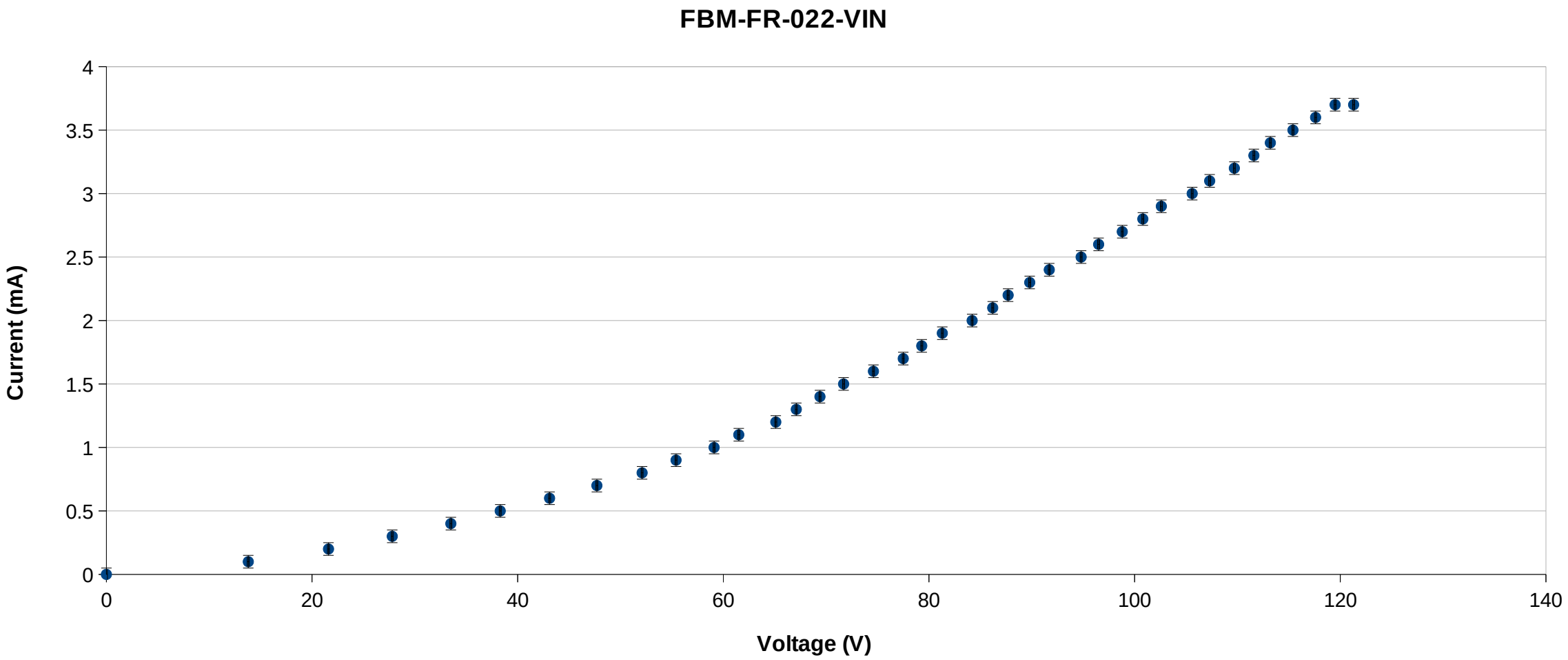
-Test: HV = (120.09 ± 0.01) V ; I = (5.9 ± 0.1) mA

Results and Analysis: Module FBM-FR-016 PRI



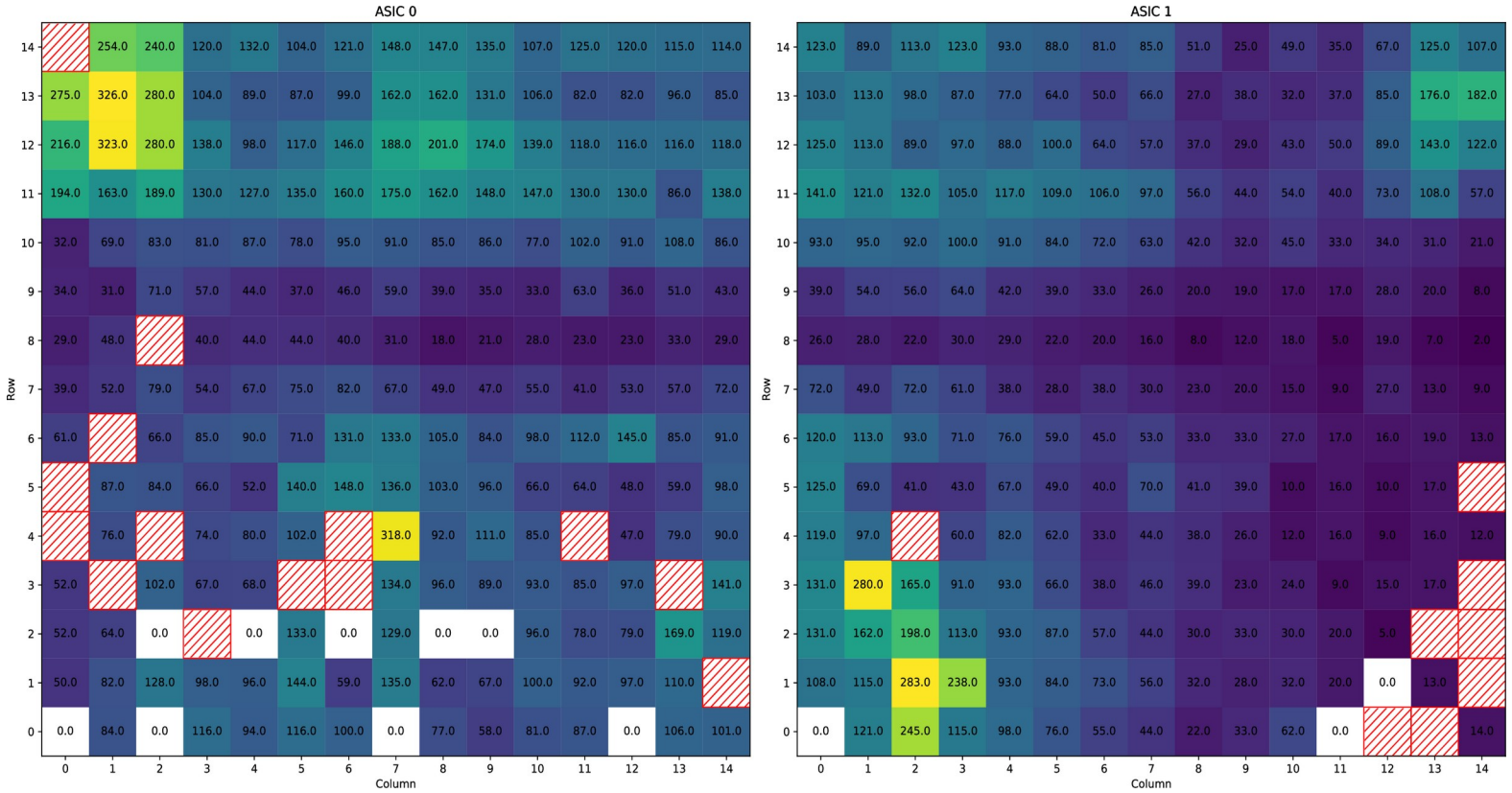


Results and Analysis: Module FBM-FR-022 VIN



Results and Analysis: Module FBM-FR-022 VIN

Bump Connectivity test (IJCLAB)



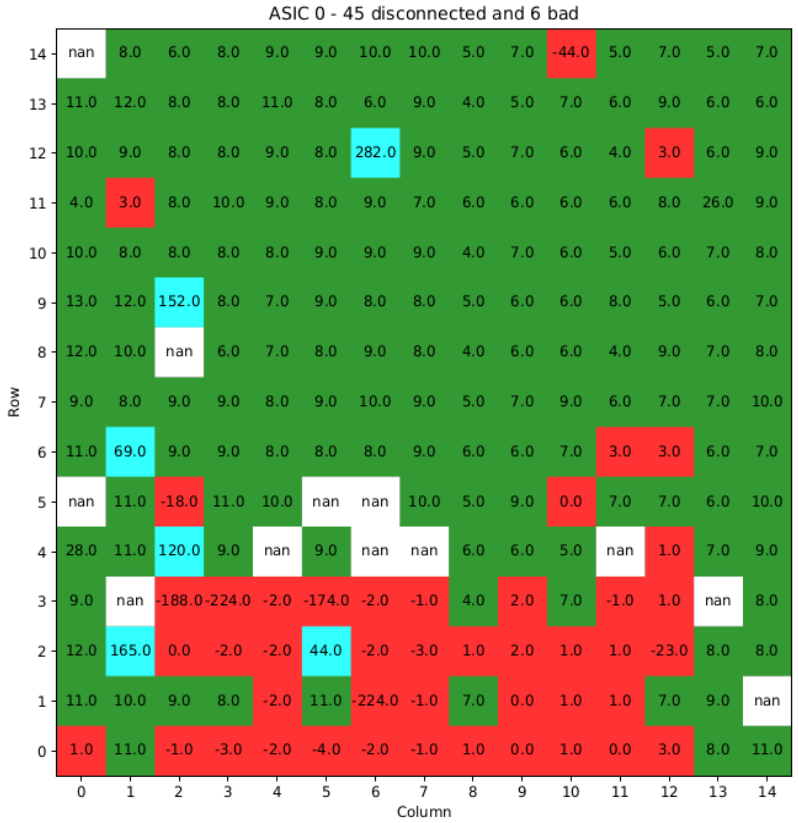
-Test: HV = (120.08 ± 0.01) V ; I = (3.7 ± 0.1) mA

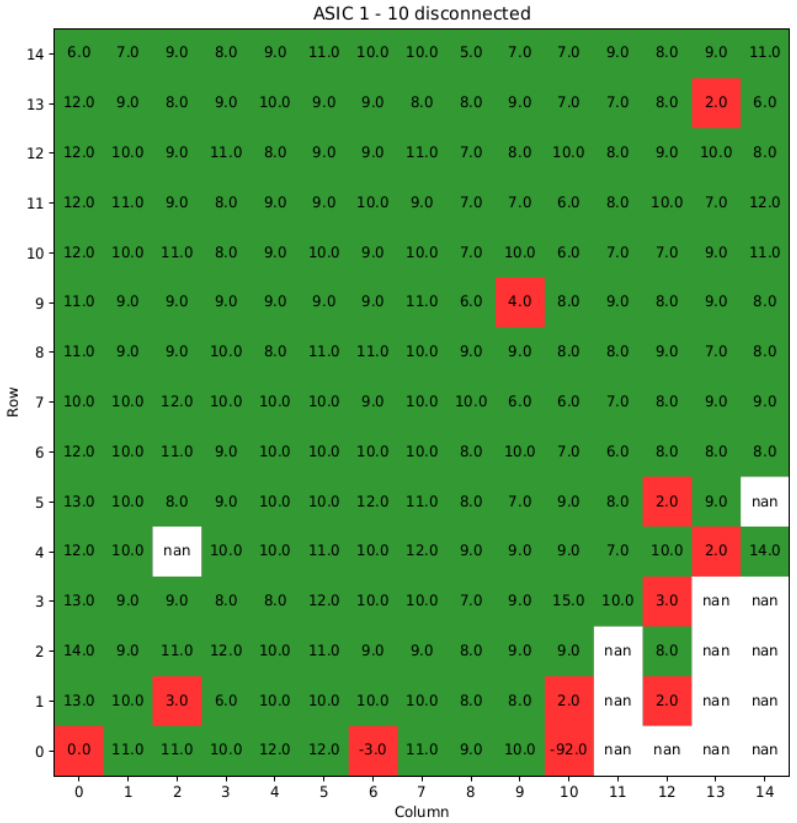
Analysis and comments:

- This test was done with a nuclear β-decay source.
- This is done inmediatly after module assambly at IJCLab
- This shows that Chip 1 (ASIC 1) is in better conditions that Chip 0, but it has many noisy pixels.

Results and Analysis: Module FBM-FR-022 VIN

Bump Connectivity test (LPNHE)



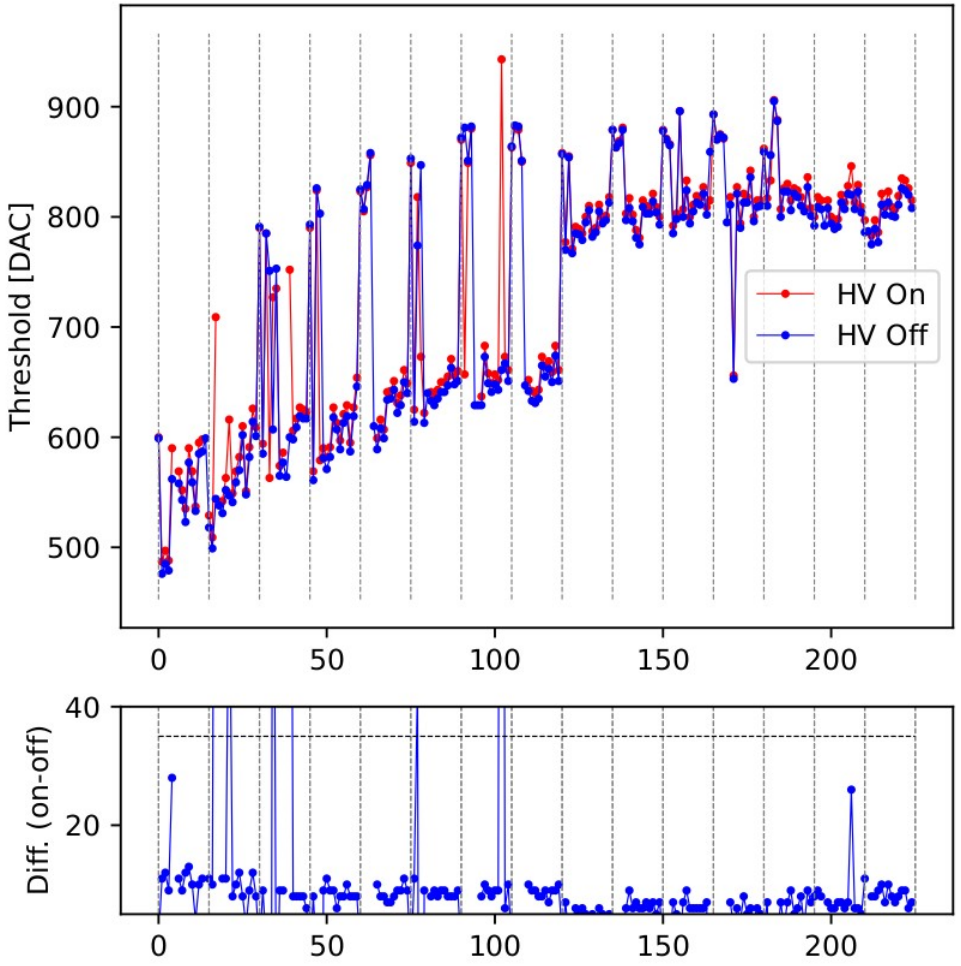


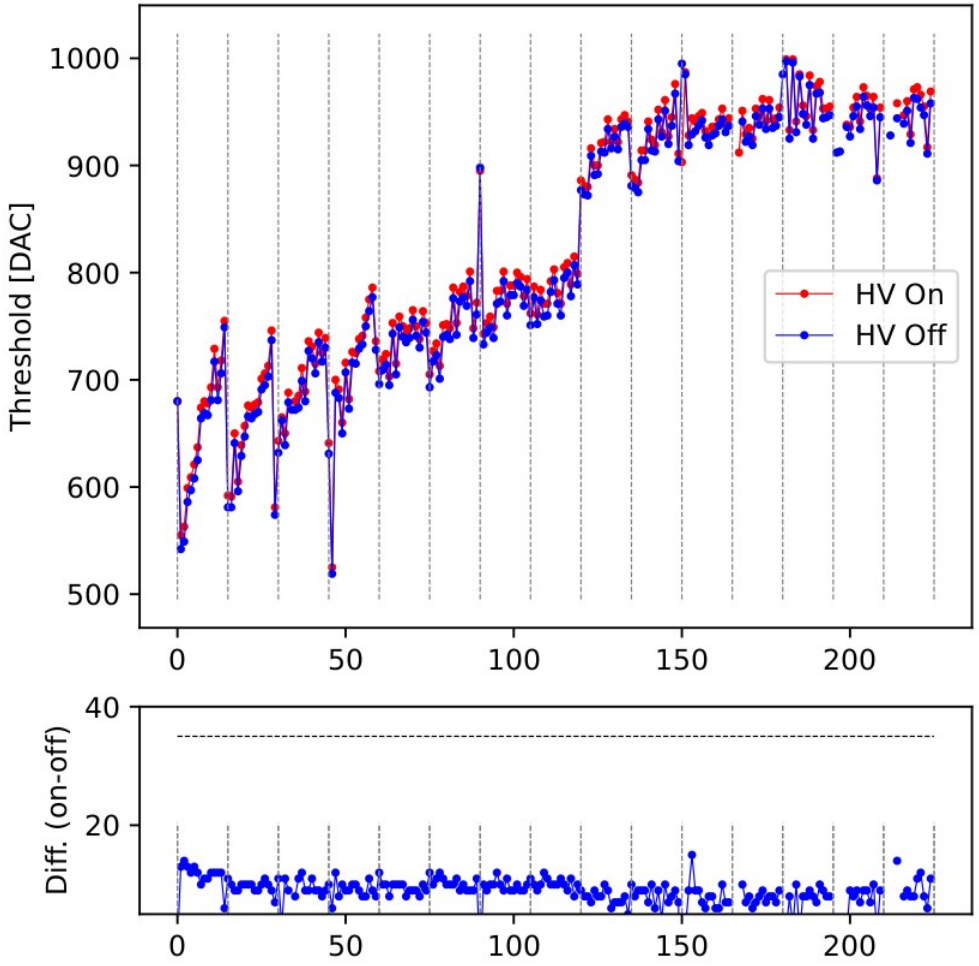
-Test: HV = (120.08 ± 0.01) V ; I = (3.7 ± 0.1) mA

Analysis and comments:

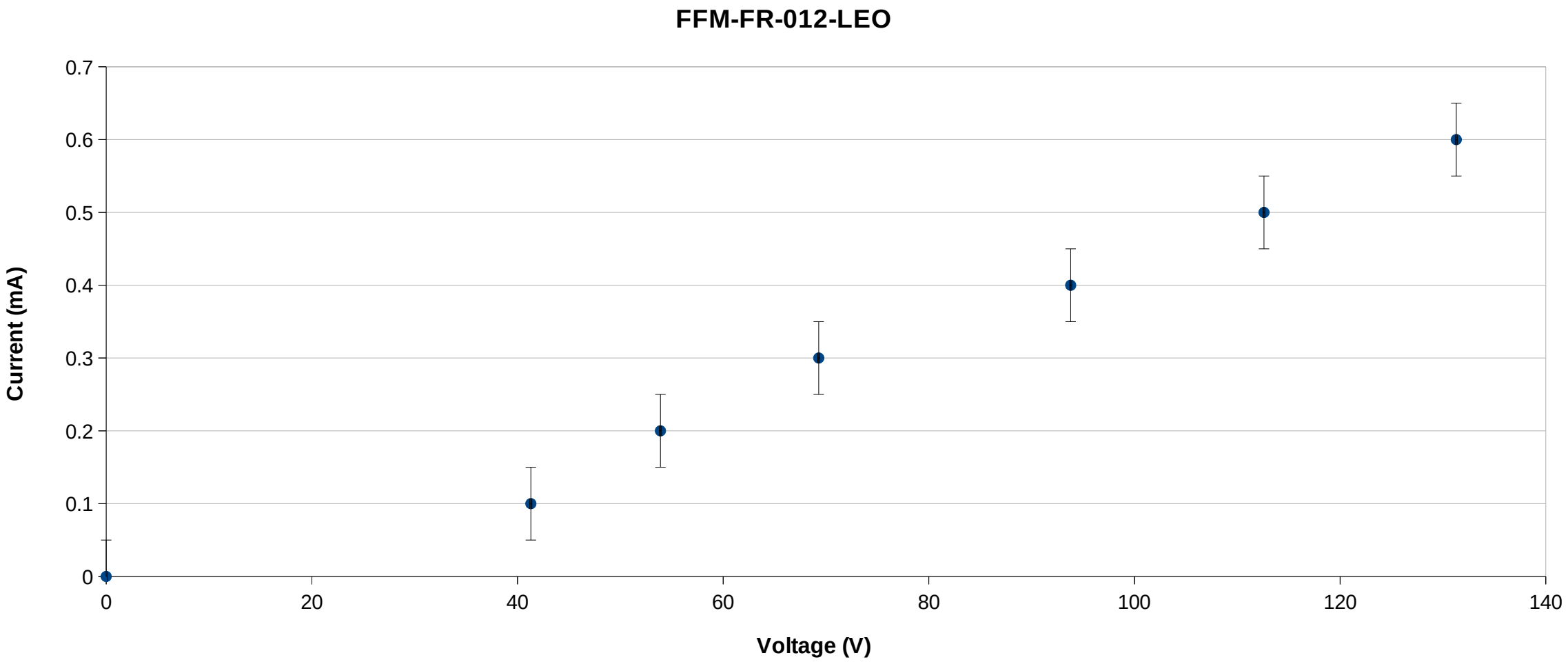
- Test shows that chip zero has a lot of disconnected pixels.
- This shows that Chip 1 (ASIC 1) is in better conditions that Chip 0, but it has many noisy pixels.
- There is a very good similarity with IJCLab test.
- This can be used in Demonstrator.

Results and Analysis: Module FBM-FR-022 VIN



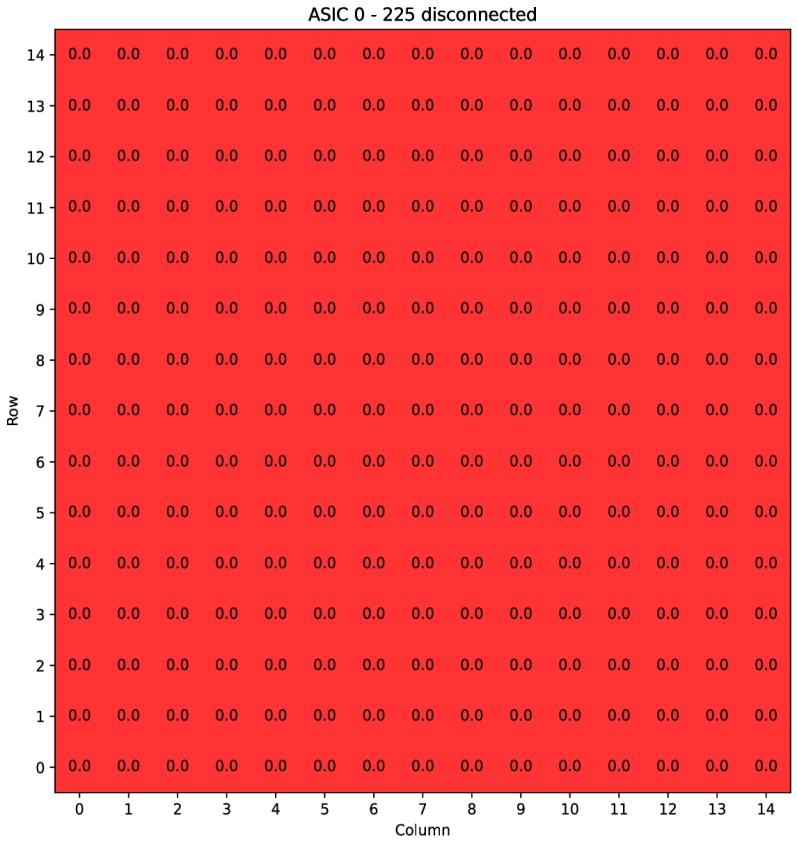


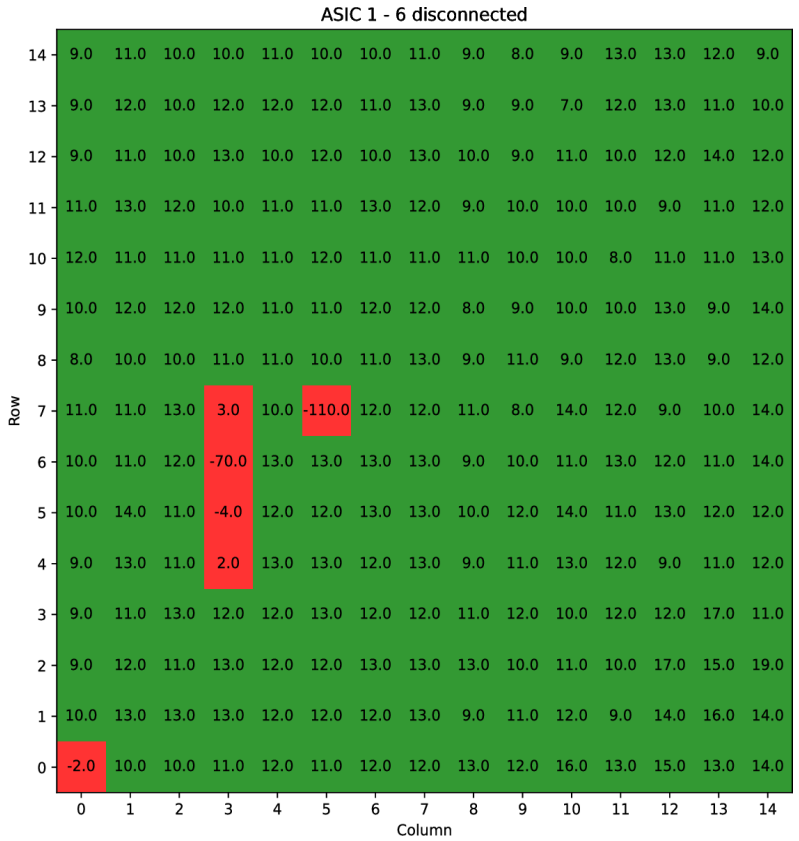
Results and Analysis: Module FBM-FR-012 LEO



Results and Analysis: Module FBM-FR-012 LEO

Bump Connectivity test (IJCLAB)





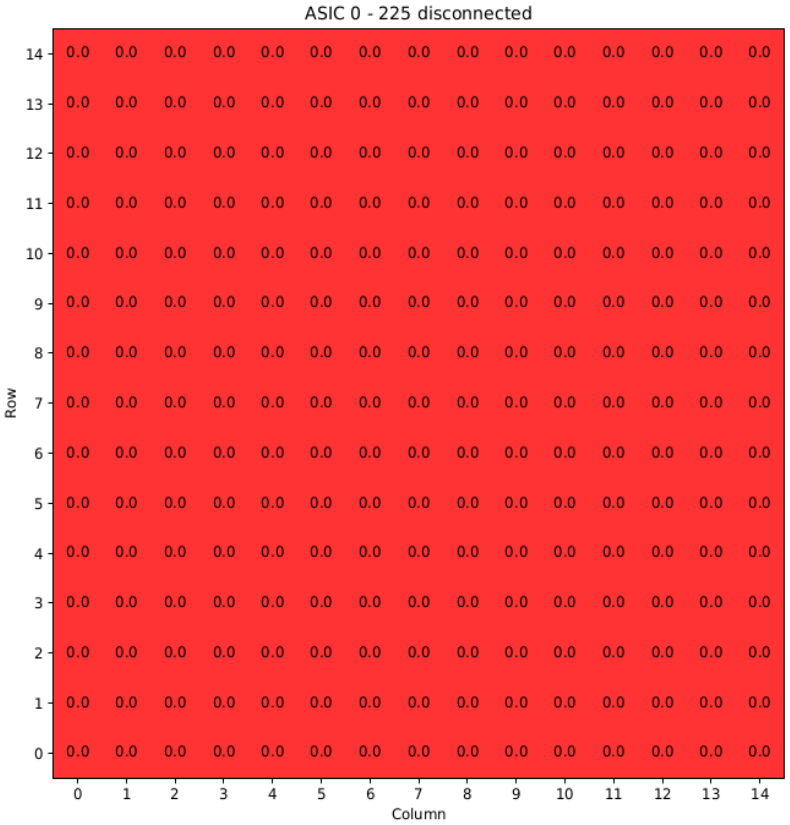
-Test: HV = (120.09 ± 0.01) V ; I = (0.5 ± 0.1) mA

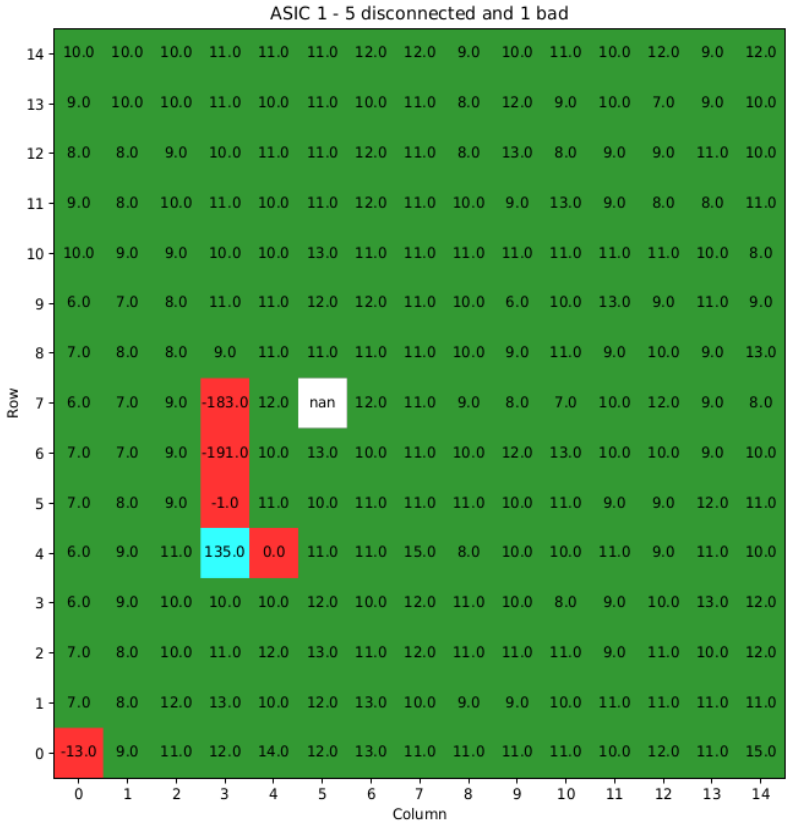
Analysis and comments:

- For this it was performed an electronic bump-connectivity test.
- The Chip zero is not useful (all their pixels are disconnected).
- Chip one can be used because It has just six disconnected pixels.

Results and Analysis: Module FBM-FR-012 LEO

Bump Connectivity test (LPNHE)



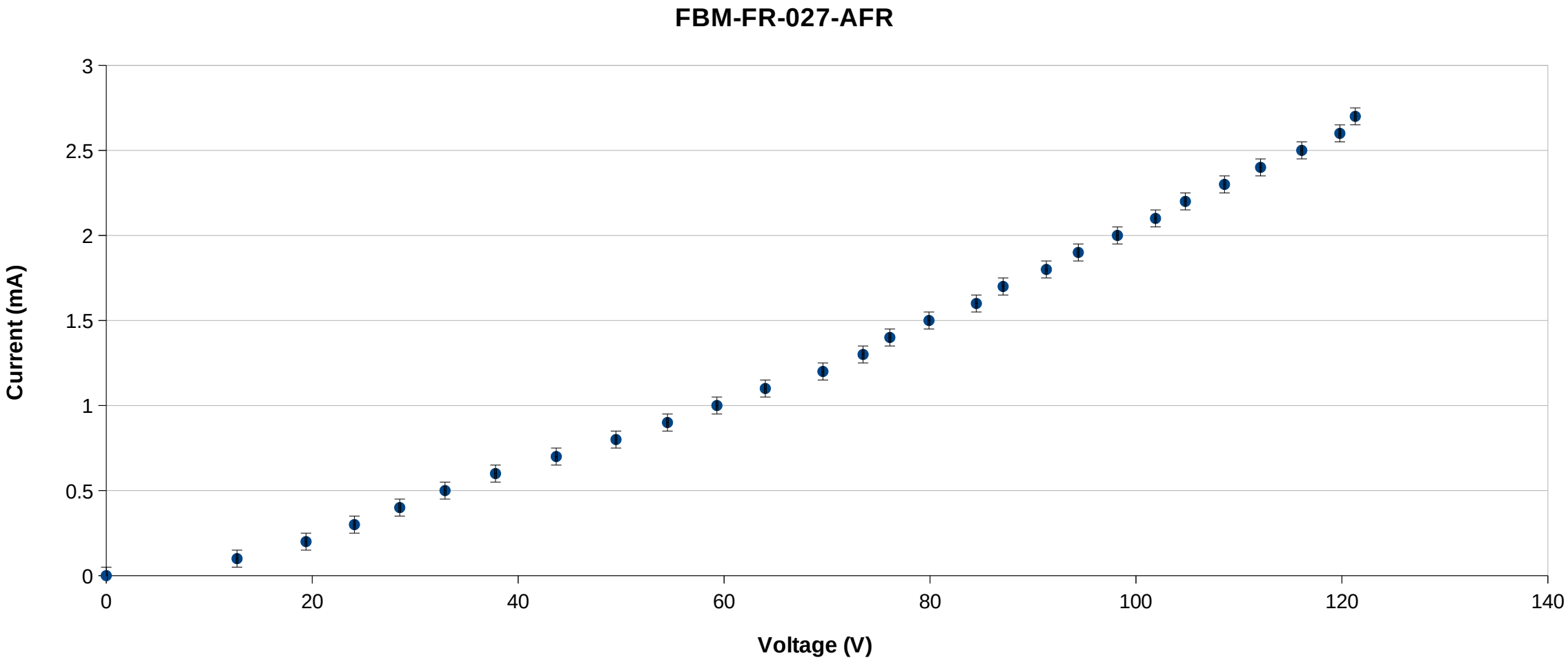


-Test: HV = (120.09 ± 0.01) V ; I = (0.5 ± 0.1) mA

Analysis and comments:

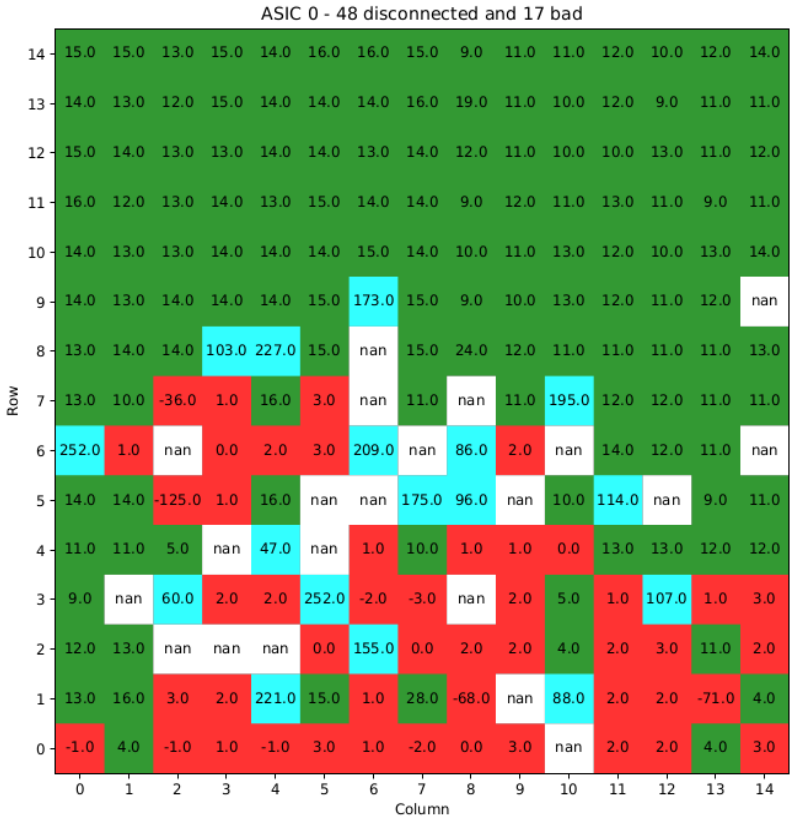
- The Chip zero is not useful (all their pixels are disconnected).
- Chip one can be used because It has just six disconnected pixels.
- There is a very good similarity with IJCLab test.
- This module will be used just for assembly studies.

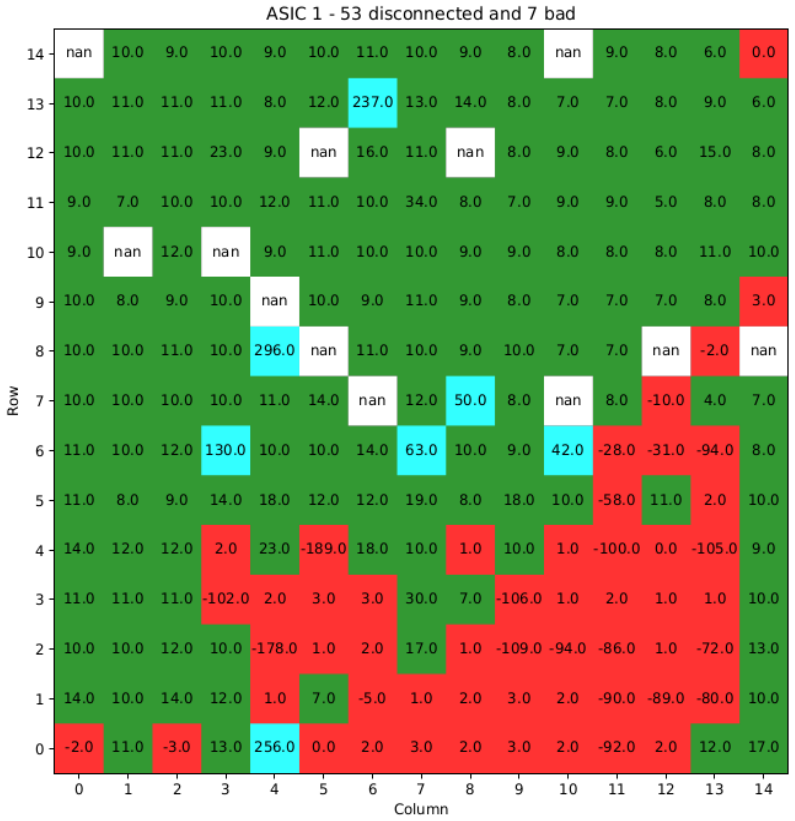
Results and Analysis: Module FBM-FR-027 AFR



Results and Analysis: Module FBM-FR-027 AFR

Bump Connectivity test (LPNHE)



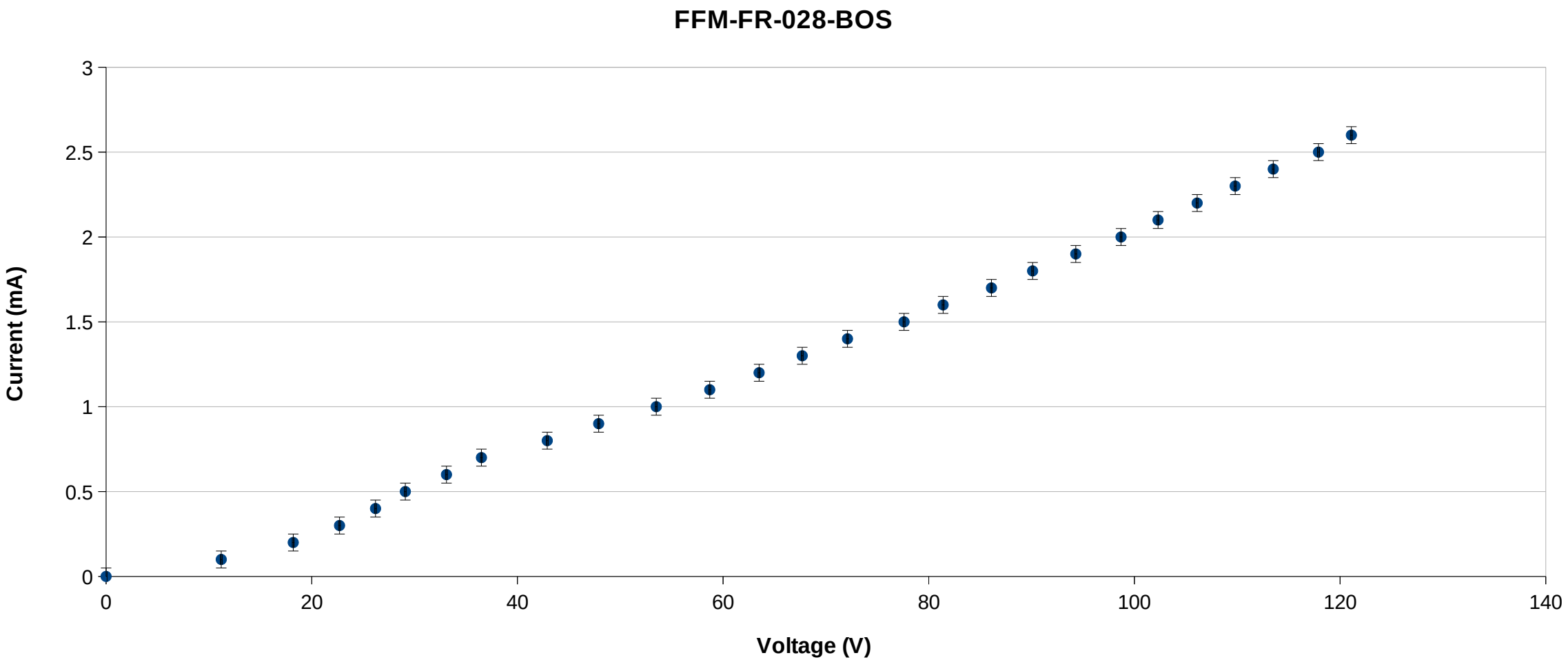


-Test: HV = (100.08 ± 0.01) V ; I = (2.6 ± 0.1) mA

Analysis and comments:

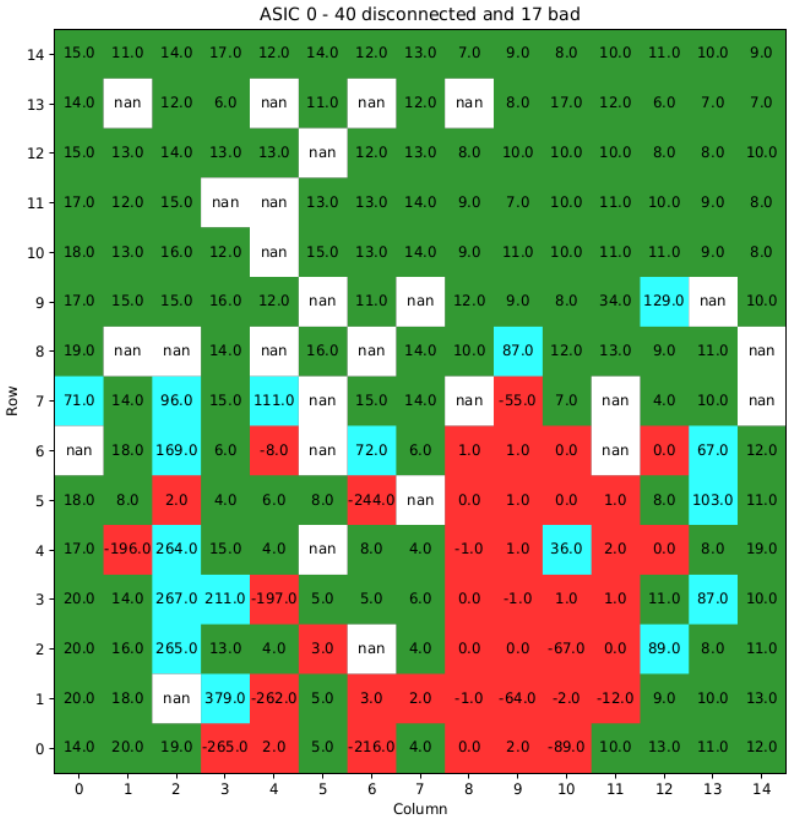
- There's no IJCLab bump Connectivity test for this module.
- There are a lot of disconnected pixels in both chips.
- The module has suffered damage.
- This can be used in Demonstrator just for assembly purposes.

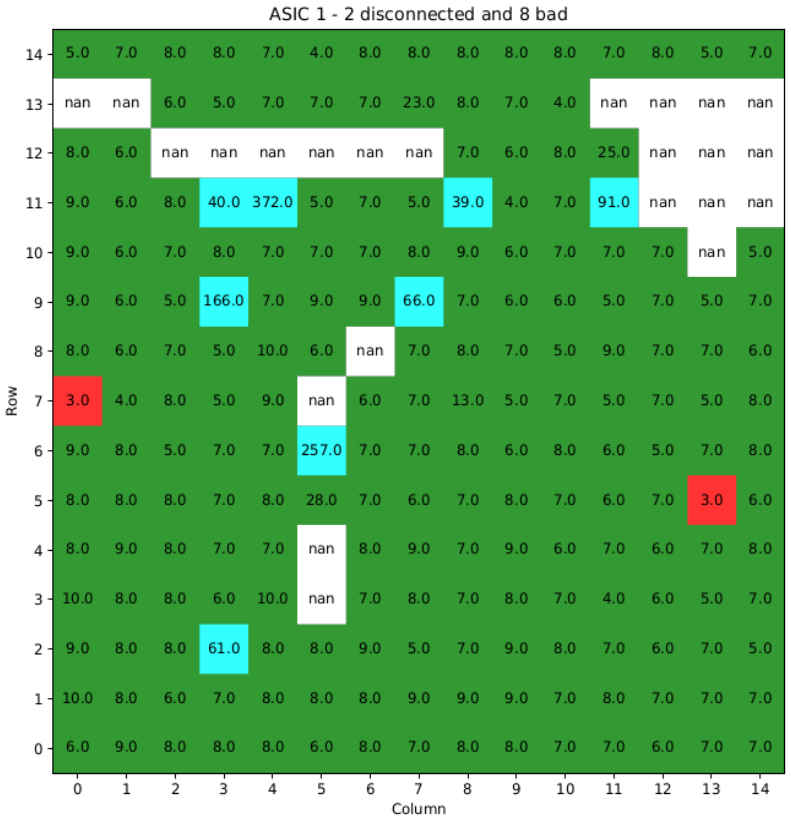
Results and Analysis: Module FFM-FR-028 BOS



Results and Analysis: Module FFM-FR-028 BOS

Bump Connectivity test (LPNHE)





-Test: HV = (120.10 ± 0.01) V ; I = (2.5 ± 0.1) mA

Analysis and comments:

- There's no IJCLab bump Connectivity test for this module.
- There are a lot of disconnected pixels in chip zero.
- There are a lot of noisy pixels in chips zero and one.
- This can be used in Demonstrator just for assembly purposes.

Conclusions

- The development of an automated electrical measurement system was achieved through the creation and use of code that executes various types of tests in modules and analyze results.

- The modules tested will be used for the HGTD demonstrator.

- The quality varies greatly from one module to another. Some will be used for all the tests at CERN and others will only be used for assembly studies (metrology and testing the flatness of surfaces in contact with the cooling plate).

- The R&D phase is essential for improving each component of the detector, including sensors, ASICs, modules, supports and detector units, and for fine-tuning procedures in preparation for pre-production and production of the HGTD detector.

- Contribution to the software of the gluing robots (current and new one). The code done provides the trajectories for the glue dispenser and enabled to make a prototype unit detector (with glass plates).

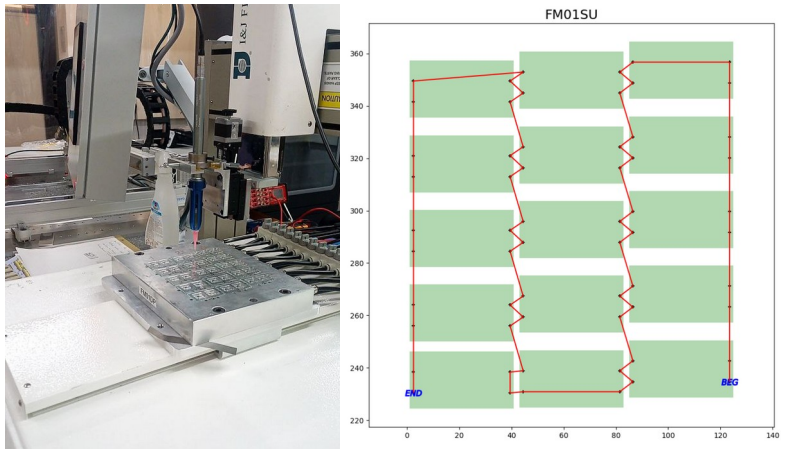


Figure 11: Gluing old Robot.

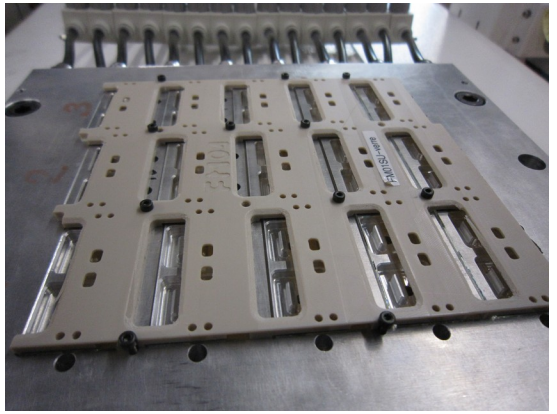


Figure 12: Prototype unit detector.

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lacongaphysics

Latin American alliance for Capacity buildiNG in Advanced physics

LA-CoNGA physics

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Back-up: ALTIROC (Experimental Framework)

- ALTIROC must also compute the number of hits on a bunch-by-bunch basis for luminosity measurement in the range of $2.4 < |\eta| < 3.5$.

- The performance of LGAD sensor is strongly correlated with the performance of the read-out ASIC ALTIROC. ALTIROC matrix consists of 15×15 channels and it is designed using the 130 nm TSMC technology.

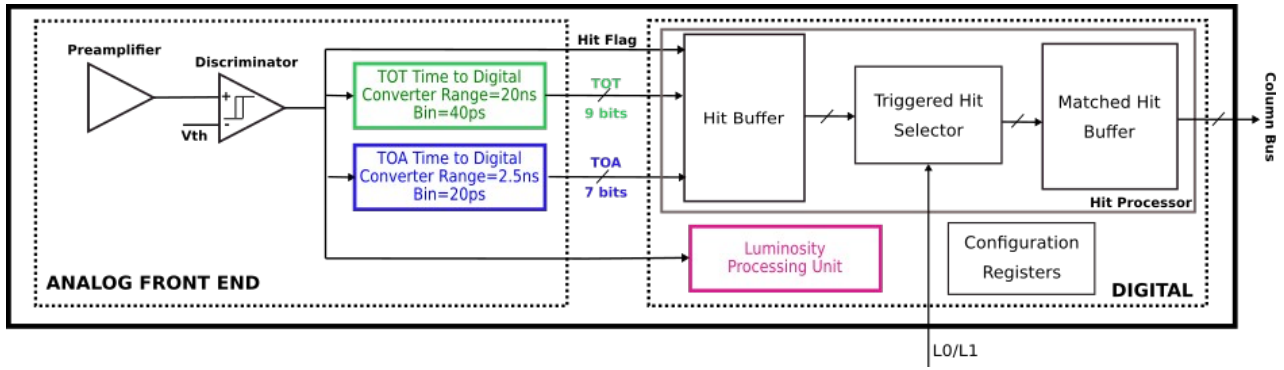


Figure 13: Diagram of an ALTIROC circuit structure.

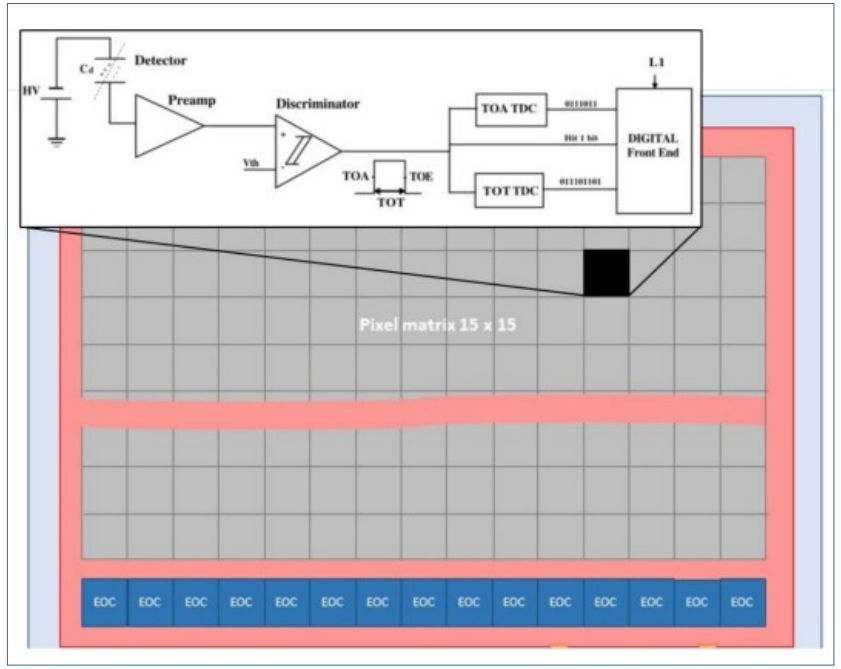
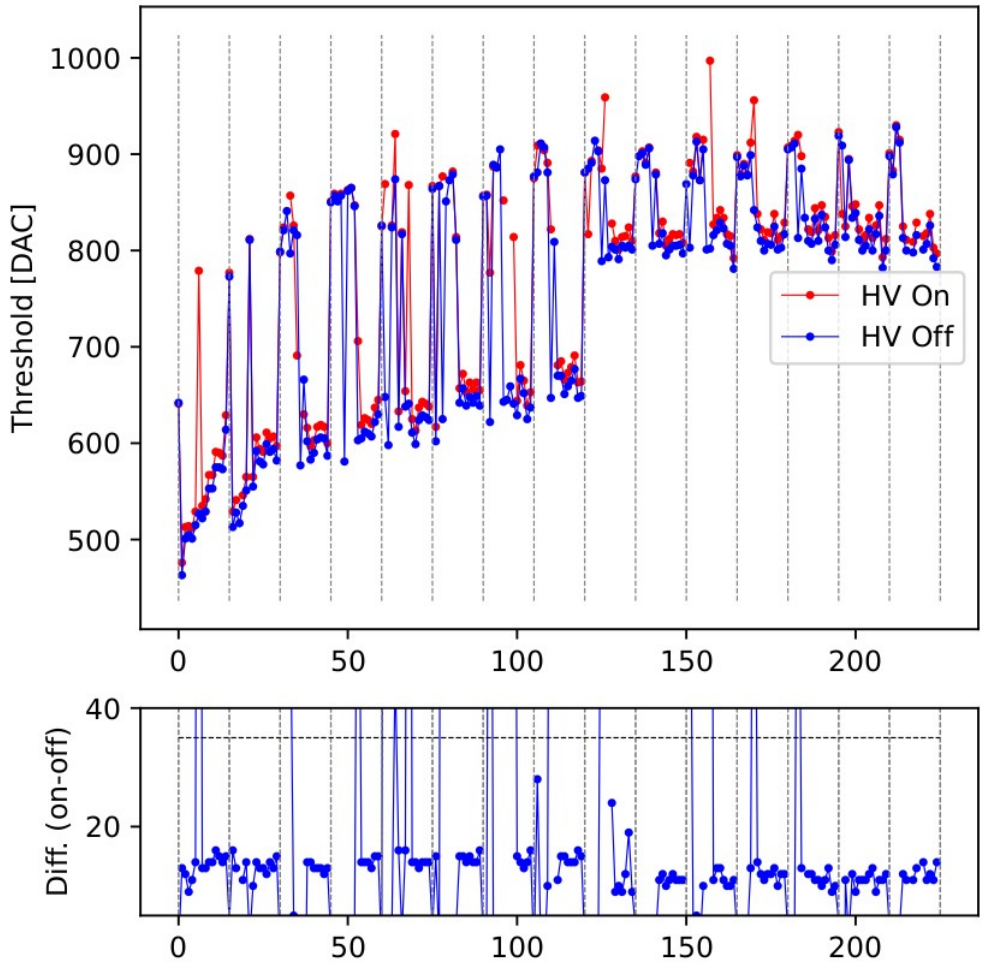
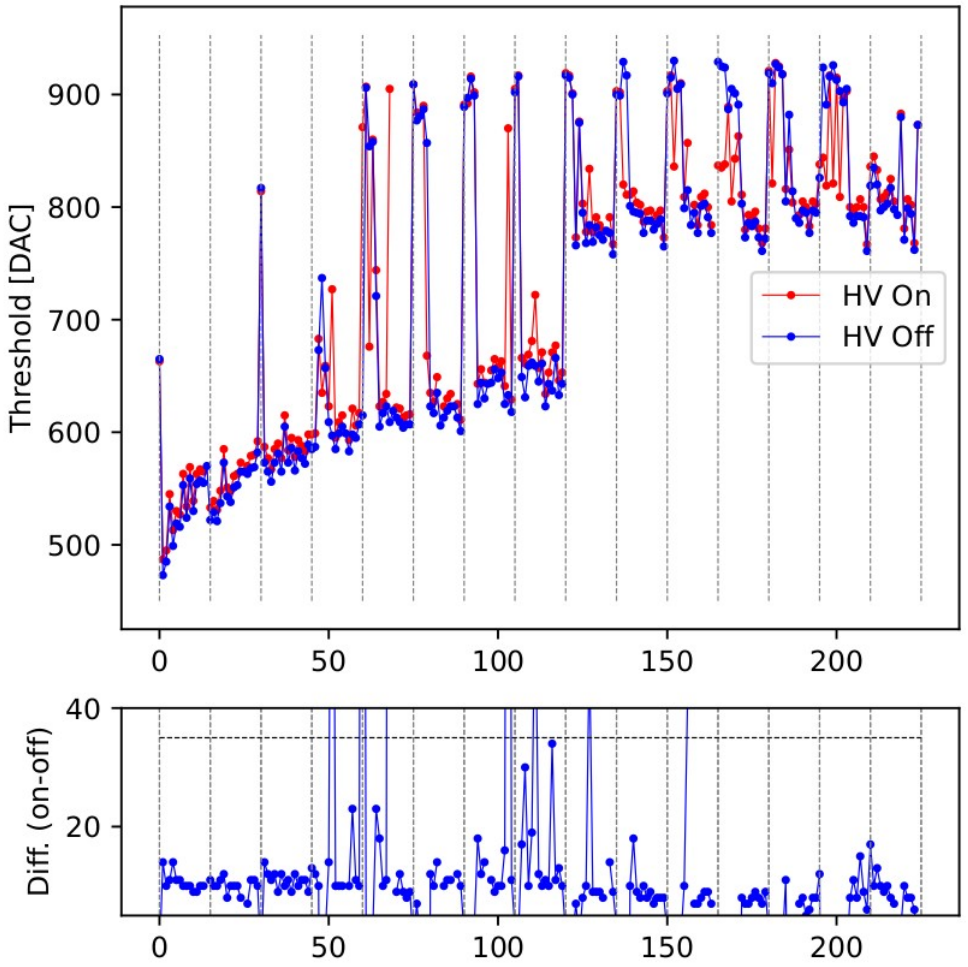


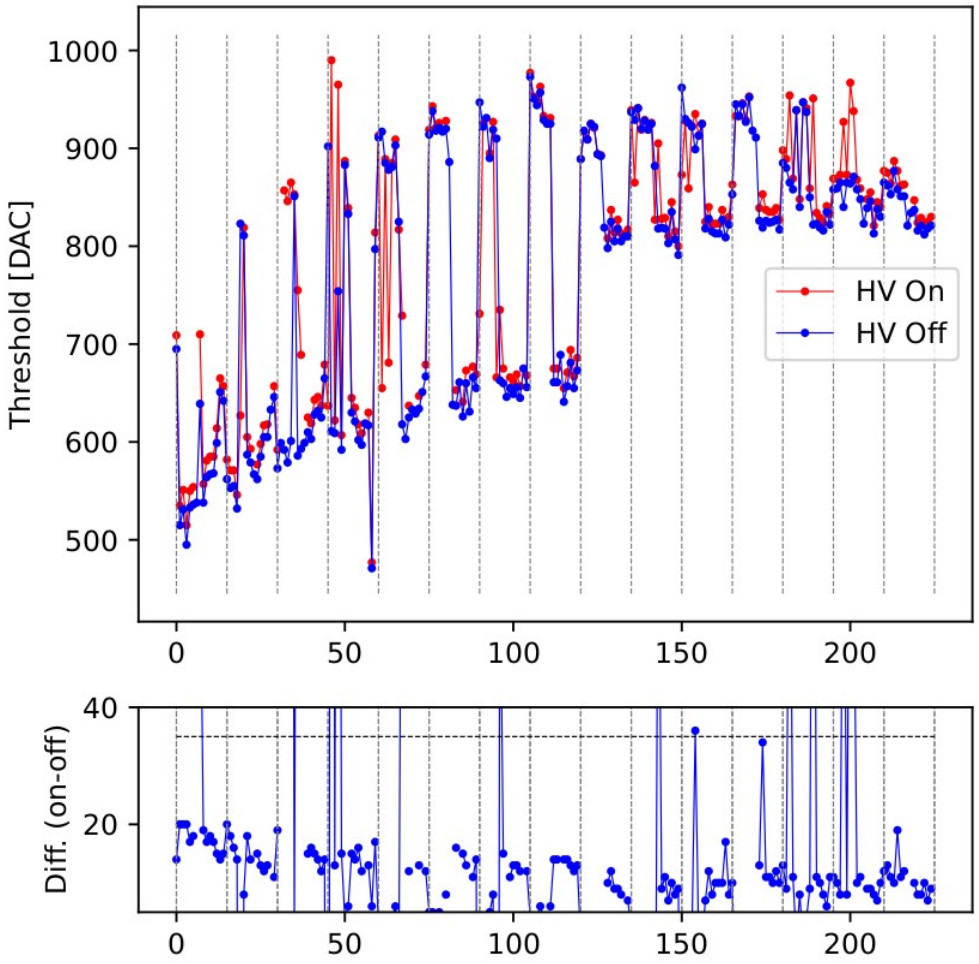
Figure 14: ALTIROC circuits incorporated in a module.

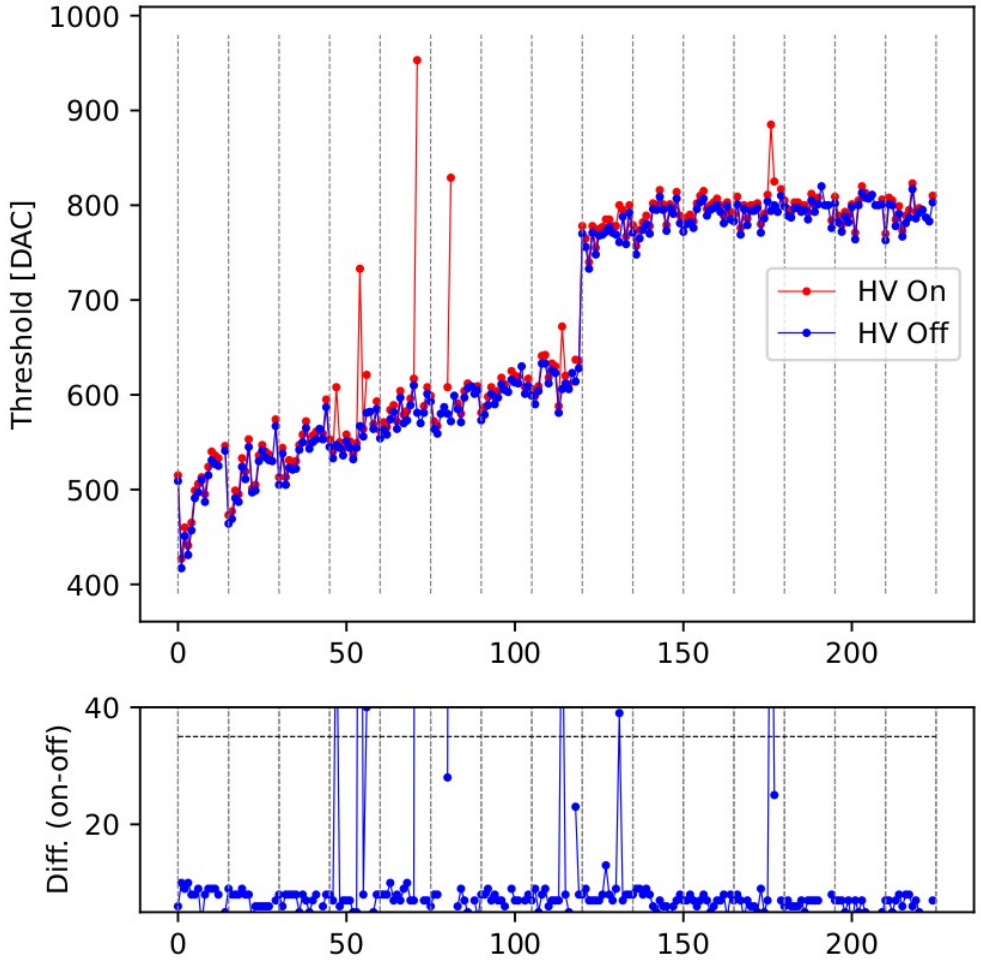
Back-up: Module FBM-FR-027 AFR (Results and Analysis)





Back-up: Module FFM-FR-028 BOS (Results and Analysis)





Back-up: Module FBM-FR-012 LEO (Results and Analysis)